SOLID-STATE IMAGE DETECTOR DEVELOPMENT:
A LINEAR DIODE ARRAY FOR ASTRONOMICAL SPECTROSCOPY

A thesis

submitted in partial fulfilment

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To Lyndy

CONTENTS

LIST OF FIGURES

FIGURE PAGE

FIGURE PAGE

FIGURE PAGE

FIGURE PAGE

FIGURE PAGE

LIST OF PLATES

LIST OF TABLES

GLOSSARY

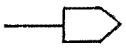
ac	alternating current (or non-zero frequencies)
A/D	Analogue to Digital Convertor
CMOS	Complementary Metal Oxide Semiconductor
CPU	Central Processing Unit
dc	direct current (or zero frequency component)
e^-/h	electron/hole
EMC	Electromagnetic Compatability
EMI	Electromagnetic Interferrence
EPROM	Erasable/Programmable Read Only Memory
DOS	Disk Operating System
DQE	Detective Quantum Efficiency
JFET	Junction Field Effect Transistor
kbyte	1024 bytes
LDA	Linear Diode Array
LSB	Least Significant Bit
MJUO	Mount John University Observatory
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
MTF	Modulation Transfer Function
PCB	Printed Circuit Board
ppm	parts per million
RAM	Random Access Memory
r.m.s.	root mean square
rti	referred to input
RQE	Responsive Quantum Efficiency
STC	System Timing Controller
swg	standard wire gauge
TC	Temperature Coefficient
UCPD	University of Canterbury Physics Department

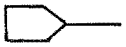
LOGIC WAVEFORMS

E	Logic waveform 'Example' which causes its action when 'high'.
$\overline{E}$	Logic waveform 'Example' which causes its action when 'low'.
E_e	Logic waveform 'Example' which causes its action with a positive going edge.
$\overline{E}_e$	Logic waveform 'Example' which causes its action with a negative going edge.
C_o	Master Clock for the shift register which reads out the odd numbered pairs of diodes.
ϕ_1	First clock for the odd shift register.
ϕ_2	Second clock for the odd shift register.
S_o	Start pulse for the odd shift register.
ROV	Reset Odd Video
C_e	Master Clock for the shift register which reads out the even numbered pairs of diodes.
ϕ_1'	First clock for the even shift register.
ϕ_2'	Second clock for the even shift register.
S_e	Start pulse for the even shift register.
REV	Reset Even Video
$\overline{SHR}$	Sample when high, and Hold when low the Reset video level for the odd shift register. (Named $\overline{SHP}$ for the even shift register.)
$\overline{SHP}$	Sample when high, and Hold when low the Pixel level for the even shift register. (Named $\overline{SHR}$ for the odd shift register)
M_1	Video Multiplexer address line 1.
M_2	Video Multiplexer address line 2.
$\overline{A}_1$	A/D convertor input multiplexer Address line 1.
$\overline{A}_2$	A/D convertor input multiplexer Address line 2.
$\overline{ADC}_e$	Analogue to Digital Convert.
$\overline{PL}$	Parallel Load the A/D data into the shift register.
$\overline{DAV}$	Data AVailable to the Data Acquisition System.
SC_e	Serial Clock for the A/D convertor data.

SYMBOLS

Circuit Diagram Symbols:


Signal input to circuit


Signal output from circuit


Continuation of signal distribution

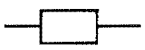
GP
Ground Plane

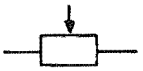

Zero signal reference (Signal ground)

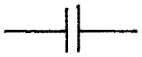

Power Earth

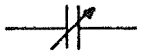

Continuation of zero signal reference

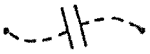
Connections to power supply


Resistor


Variable resistance


Capacitor, (optional '+' for polarity)


Variable capacitance


Stray (undesirable) capacitance

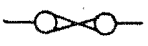

Diode


Light emitiing diode


Zener diode

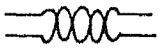

Triac

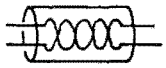

Metal Oxide Varistor

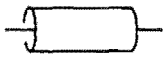

Fuse


Test point (Oscilloscope probe hook)


Mini-jump option selector

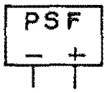

Twisted pair cable


Shielded twisted pair cable

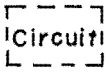

Co-axial cable

Undesirable commom-mode voltage generator

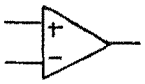

Current noise source

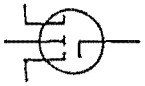


Analogue power supply filter



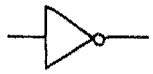
Internal representation of a component

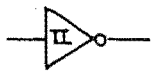

Operational amplifier (or comparator)


SD214 D-MOS switch

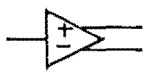

NPN transitor

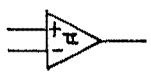

PNP transitor

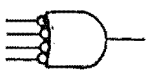

Inverting logic gate

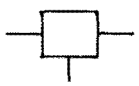

Inverting logic gate with input hysterisis

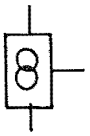

Negated AND (NAND) logic gate


Differential logic line driver

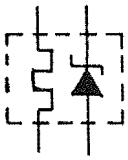

Differential logic line receiver


Quad input active low or gate

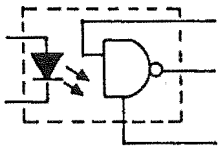

Three terminal voltage regulator



LM334 constant current source



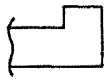
LM339 precision voltage reference



HP137 optical coupler

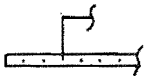
Printed Circuit Board Symbols:

1.0 mm diameter signal path



Wide track for high current paths

Connection of component to PCB GP



Rogers Q/PAC dual strip transmission line

Resistor (or polystyrine capacitor if big)

20 turn variable resistor

Zero ohm jumper

MKT1817 100 nF 63V capacitor

Tantulum capacitor

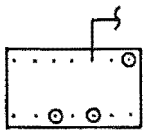
MKT 1818 (or 1822) Polypropylene capacitor

Variable capacitor

1N4007 diode

Mini-jump (3-pin in example)

Test point (Oscilloscope probe hook)



Plastic or ceramic packaged integrated circuit in socket. Free 'dots' indicate pins connected to ground plane, circled dots indicate unconnected pins.

TO99 metal can packaged integrated circuit in socket.

Medium power transistor

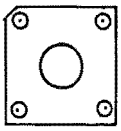
LM339 precision voltage reference

SD214 D-MOS switch

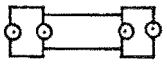
LM134 constant current source

LM185-2.5 volt zener reference diode

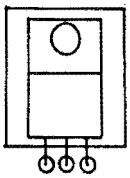
Connhex 50 Ω co-ax receptacle



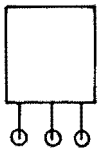
Diode bridge (3 A per leg)



Fuseable link in holder



TO-220 packaged 3-terminal regulator or triac



Right-angle Molex connector (3-pin examale)

Straight Molex connector

ABSTRACT

Future spectroscopic observational programmes at Mount John University Observatory require the ability to acquire spectra with significantly higher spectrophotometric accuracy and geometrical stability than can currently be achieved. Therefore a solid-state linear-diode-array image detector system has been designed and developed for use with the MJUO échelle spectrograph.

A review of those electromechanical design techniques of significance to astronomical instrumentation is presented. Their application is exemplified with a complete electromechanical design for the detector, which is found to allow each electronic sub-system implemented within that design to achieve its theoretical level of performance.

The requirements for the video processing electronics of a solid-state image detector are explicitly developed, and are used to design the electronics for this detector. Subtle sources of electronic instability which can appear as noise or base-line shifts are identified and controlled in this design. In particular, differential non-linearity is identified in an existing preamplifier design, and so an alternative design is implemented.

The readout noise of the entire detector system is measured to be 200 e^-/h pairs for a noiseless signal source of zero impedance to ground. This increases to 350 e^-/h pairs when the impedance of this source is equal to that of the diode array, due to an additional noise contribution of 290 e^-/h pairs. The net readout noise with the RL936F/30 diode array is 450 e^-/h pairs, which is the quadratic sum of the detector system noise with the two 210 e^-/h pair samples of diode capacitance thermodynamic noise. Thus the diode array is not found to contribute any noise in excess of its theoretical thermodynamic noise.

A temperature controller is developed for use with sensors which are cooled in cryogenic dewars. A short term control precision of 1.6 mK r.m.s. is achieved which is entirely due to the theoretical noise of the temperature sensor. The long term precision over all operating conditions

is ±20 mK, which is dependent on the design of the dewar.

The hardware and software which provide interactive instrument control and data reduction are described. In particular, they provide for flexible control of the detector sub-systems during data acquisition and testing, and enable a high level of data reduction to be undertaken while the detector is integrating.

An observational programme has been carried out with this detector system on the southern RS CVn system HR4492. Radial velocity measurements with a precision of ±0.5 km s^{-1} have enabled a new ephemeris for the binary motion to be determined, namely HJD = 2446317.5 ± 21.82E. It is used to interpret Hα line profile variations in terms of probable mass transfer within the system.

INTRODUCTION

For an overall understanding of the chemical and dynamical evolution of our Galaxy, the physical and chemical properties of its components have to be deduced. This may involve a wide range of observational work (for example, on the interstellar medium or individual stars in both the disk and halo populations), laboratory work (for example, on line oscillator strengths or chemical reaction rates), and theoretical work (for example, stellar structure and evolution). As part of the observational work, there are many astrophysically interesting research areas (for example isotopic ratios, stellar radial velocities, and line profile analysis), which require the use of detectors capable of obtaining data with signal-to-noise ratios significantly higher than 100:1, and with correspondingly high spectrophotometric accuracy.

Griffin's (1968) use of photographic plates as a detector has shown that it is extremely difficult to calibrate their non-linear response to a spectrophotometric precision of better than 1% for even the brightest stars. Therefore during the last decade, a number of research groups have developed solid-state detector systems to address specific astrophysical problems which require higher signal-to-noise ratios and spectrophotometric accuracies than can be achieved by photographic plates.

The McDonald Observatory system (Vogt, Tull, and Kelton 1978) has been used extensively by Lambert and his colleagues for stellar atmosphere analysis using weak line equivalent widths (see for example, Sneden et al. 1981, and Dominy et al. 1978), and for identifying the secondaries of spectroscopic binaries (see Tomkin 1978). High quality data obtained with a similar system at the European Southern Observatory coudé auxillary-feed telescope, has, for example, been used by Federman et al. (1984) to observe weak interstellar features, and by Lambert and Danks (1985) to observe the weak helium D_3 line in late-type stars. This latter work illustrates the ability to precisely remove the telluric lines from a spectrum by dividing it with the spectrum of a stellar continuum

source. Gray (1982a,b) has extensively analysed line profiles in stellar spectra to obtain their rotation and turbulence information, and thereby identify a dynamo rotational braking mechanism in stellar evolution. Additional line profile data from his system at the University of Ontario (Gray, 1986) are leading to an understanding of the turbulent motions within stellar atmospheres. Vogt (1982) has developed a system at Lick Observatory which he has applied to Doppler imaging of starspots in chromospherically active stars (see Vogt and Penrod 1983). Finally, Campbell et al. (1979, 1981) has introduced an hydrogen-fluoride cell into his optical path in an effort to measure radial velocities with the extremely high precision of $\approx 10\ ms^{-1}$. In common with the work of Gray is the demonstration of high geometrical stability in their systems.

Of revolutionary significance to observational astronomy are the various solid-state image detectors. Indeed, the above examples have been undertaken using a self-scanning linear diode-array sensor. While this thesis will concentrate on this type of detecting element, a discussion of other types of solid-state detectors used in astronomy is given by Timothy (1983), and in references therein.

This thesis is organized to give the reader a thorough development of the total concept involved in the design, construction, and use of a Linear Diode Array detector for high resolution stellar spectroscopy.

In order to discuss any solid-state detector system, the terminology and basic definitions required need to be introduced. These will be given in Chapter 1, and will include the response of the detector to illumination, its sources of noise, its dynamic range, and its efficiency. The linear diode array detector will be described in Chapter 2. In particular, details of its operating environment, and the method by which data is retrieved from the detector are given. In addition, the basic ideas raised in Chapter 1 are specifically addressed in relation to the linear diode array. Most of the material in these two chapters has been developed from a wide variety of reference material. It is therefore difficult to reference a single text or publication which describes all the features which need to be addressed.

Having selected a detector, the rest of the instrument package must be designed to produce an integrated physical system. In Chapter 3, the requirements for the underlying electromechanical design of that system are determined, and the techniques for achieving them are reviewed. Specific details of its implementation in the Mount John University Observatory LDA system are given there, and also in Chapter 4. This latter chapter also deals with the cryogenics, as well as the justification for, and the means by which the temperature environment is controlled.

Chapters 5 and 6 determine the requirements and designs the electronic sub-systems which process the video signal and control the array. Given their implementation within the electromechanical design, this process need only consider the circuitry requirements of those electronics. Careful attention to detail enables many subtle sources of noise and instability to be identified and minimized.

The acquistion and reduction of the digital data, for which this whole system was designed and intended, is outlined in Chapter 7. It gives a description of the Data Acquisition System hardware, and of the software options which are available for performing these tasks.

Finally, the ultimate proof of the performance of any system is how it performs on the astronomical instrument and in the working environment for which it was intended. In spite of electrostatic discharge damage that existed in the diode array chip for this system, a number of moderate quality spectra of the chromospherically active HR4492 system are able to be given in Chapter 8. They are used to derive a new orbital period and ephemeris for HR4492, as well as to detect both the helium D_3 and Li I 6707Å features. Variations in the line profile of Hα are reduced from the spectra, and are interpreted in terms of possible mass transfer within the system.

The number of tests which can be meaningfully made of the performance of this detector system is currently limited by the electrostatic discharge damage to the diode array chip. Therefore, a number of additional tests, to be performed when the new Reticon RL1872F/30 diode array is implemented, will be given in Chapter 9.

The electronic and geometrical stability of this instrument will allow many new astrophysical problems to be carried out at Mount John University Observatory. They will include weak line abundance and isotopic ratio work, monitoring of subtle line profile variations in a variety of stars, and the measurement of high precision radial velocities.

CHAPTER ONE

CHARACTERISTICS OF SOLID-STATE DETECTORS

An astronomical instrument is optically configured so that it collects the quanta of electromagnetic radiation from its target, and images them onto its image detector in a desired representation. The image detector is a device that captures photons that are incident upon it, and converts them into a recordable form. The desirable properties of this detector include the following.

1) A large portion of the image produced by the optical configuration of the instrument can be imaged onto it.

2) It converts a high proportion of the photons that are imaged onto it into recordable form.

3) It operates over a large range of photon arrival rates.

4) The incident image is reliably and precisely calculable from the recorded signal.

5) It is operationally simple, reliable, and robust.

Of revolutionary significance to observational astronomy is the solid-state group of image detectors.

A solid-state image detector collects photons from the spatial pattern of illumination incident upon its surface, and converts them into a voltage waveform which is a discretely sampled, ordered, sequential representation of the incident radiation pattern. The collection process is referred to as an integration, the voltage waveform is referred to as a video signal, and the discrete samples in the waveform correspond to individual picture elements called pixels. The mechanism for producing the time-varying video signal is referred to as scanning, and the scanning function is accomplished by the application of one or more electrical signals which produce the ordered sampling of the pixels. The technique of converting the video signal into recordable numbers, which represent the number of photons detected by each pixel, is called video processing. The resulting array of numbers is referred to as a frame, and in the general case, the units of those numbers will be called video processing units, VPUs. The extraction of a frame from the detector is referred to as

a readout, and that event signifies the end of the integration interval for that frame.

1.1 Photometric Transfer Functions

The photometric transfer function of a specified pixel is that function which specifies the recorded signal of the pixel for a given input illuminance. If the transfer function is the same for all pixels, it is said to be homogeneous over the detector format. A transfer function is said to be homologous over the detector format if it has the same functional form for all pixels.

1.1.1 Two-parameter Linear Functions

It is scarcely to be hoped that a detector system with more than one pixel can have a homogeneous transfer function, but a multi-pixel system can realistically be specified to have a homologous transfer function. This is truly desirable as the procedures for determining the transfer function and for performing the corresponding photometric correction separately for every pixel in the format could be formidable. The most desirable homologous pixel transfer function has a linear two-parameter functional form; one additive parameter representing the photometric zero point of the pixel, and one multiplicative parameter specifying the relative photometric sensitivity of the pixel. Equation 1.1 expresses this for detector pixel 'i' in terms of the signal S_i gain FF_i, and zero point FP_i, for a response R_i as

$$R_i = S_i FF_i + FP_i \ . \qquad (1.1)$$

The response of the detector to the absence of any signal ($S_i = 0$, for all i) is called the fixed pattern, and gives the zero point of every pixel. Therefore if the fixed pattern is subtracted from the response of the detector to uniform illumination (S_i = constant, for all i), the resulting frame called the flat field will explicitly give the relative response of every pixel. Thus if the fixed pattern and flat field have been determined, the response of the detector to any arbitrary illumination pattern can be transformed into a

pattern of relative intensities by subtracting the fixed pattern and then dividing by the flat field.

1.1.2 Photometric Non-Linearity

It is normally considered a performance irregularity if the fixed-patterned response is not linearly related to the input signal. Small deviations from linearity can be easily corrected if the system transfer function is homologous over the detector format, and has the following functional form

$$R_i = S_i\ FF_i + NL(R_i - FP_i) + FP_i \ . \qquad (1.2)$$

The error function $NL(R_i - FP_i)$ has in general a non-linear dependence on the fixed-patterned signal level, and is assumed to be homogeneous over the detector format. As illustrated in figure 1.1, it can be determined from a plot of the fixed-patterned response versus signal level by fitting a linear curve with the smallest peak-to-peak deviation from the data.

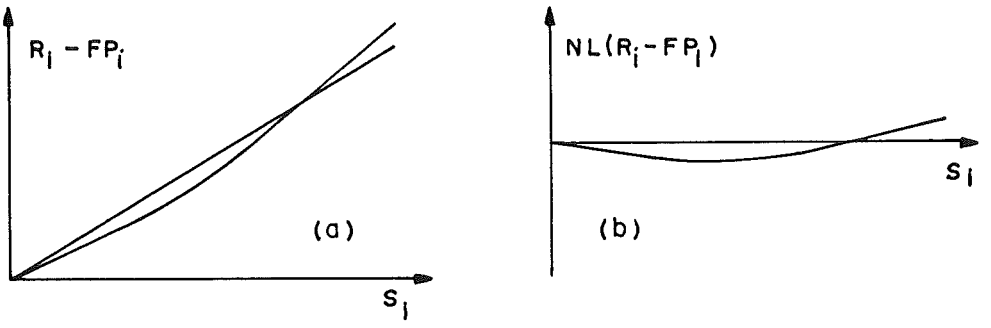


Figure 1.1: Plot showing (a) the best linear fit to the detector response, and (b) the non-linear error function for this response.

The fitted curve is assumed to be the linear term S_iFF_i, and the difference between this curve and the data curve is therefore the required error function. Thus the response to an arbitrary illumination pattern is transformed onto a linear scale of relative intensities by subtracting the appropriate non-linearity error after the fixed pattern subtraction and before the flat field division. The uniform illumination response to be used as that flat field must first have its non-linearity errors subtracted after it is fixed patterned.

1.2 Detector Output Noise

Any random fluctuation causing uncertainty in the representation of an input signal by a detector is called noise.

1.2.1 The Signal-to-noise Ratio

The precision with which the signal recorded by a detector can represent the actual signal of the illumination pattern is dependent on the net noise, and is quantified as the quotient of the recorded signal level and the noise level, called the signal-to-noise ratio. The signal-to-noise ratio can be specified for the signal from an individual pixel, or to the amplitude of an image feature spread over many pixels. An alternative interpretation of the signal-to-noise ratio is that it specifies the information content of the signal under analysis.

1.2.2 Noise Characteristics and Sources

The probability distribution of noise amplitudes is described by Poisson statistics because of the random nature of the quantum events causing noise. However in describing classical systems, the number of events causing the observed noise is so large that the skewness and kurtosis of the Poisson distribution is negligible. Therefore the noise amplitude probabilities can be well approximated by a continuous Gaussian distribution with the same variance as the underlying Poisson distribution.

If the net noise of a system is contributed to by more than one mechanism, it is well known that the instantaneous noise is the sum of the noise amplitudes of the individual mechanisms. Also, the amplitude distribution of the net noise is the convolution of the noise distributions of the individual mechanisms. As the convolution of N Gaussians with standard deviations $\sigma_i (i=1..N)$ is also a Gaussian, the net noise is described by a Gaussian of standard deviation

$$\sigma = \left[\sum_{i=1}^{N} \sigma_i^2 \right]^{0.5} \qquad (1.3)$$

where the σ_i are the individual mechanism standard deviations.

The sources of noise contributing to the net output noise of each detector pixel can be grouped into the following three categories.

1) Optical signal noise: the detected optical signal of N_p randomly arriving photons has a noise standard deviation of $\sqrt{N_p}$ photons according to classical Poisson statistics. This signal is the sum of the source and background signals in the general case, and the noise mechanism is referred to as shot noise.

2) Dark signal noise: signal that is detected in the absence of an optical signal is called the dark signal, and has an electronic origin within the sensor. If the dark signal amplitude is equivalent to N_d detected photons, the shot noise of this signal is $\sqrt{N_d}$ photons.

3) Readout noise: the uncertainty with which the scanning and video processing electronics can measure the signal is called the readout noise. Its standard deviation is expressed as an equivalent number of photons, σ_r, and is independent of the signal level.

Therefore the net readout frame noise of a pixel with readout noise σ_r, that collected N_p signal photons, and N_d dark equivalent photons, is found from equation 1.3 to be

$$\sigma_n = \sqrt{\sigma_r^2 + N_p + N_d} \qquad (1.4)$$

The photometric transfer function must be applied to this frame to determine the image frame.

1.2.3 Transfer Fuction Augmented Noise

Both the fixed pattern and flat field frames have an associated noise, and hence applying them to the image readout frame for correcting the photometric response of the detector, will contribute to the noise of the corrected image frame. The noise amplitude for each frame that is used or generated by the correction process can be found as follows.

Fixed pattern frames: The required integration time to acquire a fixed pattern frame could theoretically be zero because there is no photon flux, $N_p = 0$, to be integrated. Thus only a negligible dark signal, $N_d \approx 0$, can be accumulated in the short fixed pattern integration time, and therefore it follows from equation 1.4 that the noise of a single fixed pattern frame is equal to the detector readout noise. However consider a numerically generated frame which is the average of n_{fp} fixed pattern frames, called an averaged fixed pattern frame. The signal component of this frame is unchanged from that of any individual frame, whereas the noise component found by first using equation 1.3 for the sum of the noises, is

$$\sigma_{fp} = \frac{\sigma_r}{\sqrt{n_{fp}}} \tag{1.5}$$

Thus the noise of an averaged fixed pattern frame can be made smaller than the noise of the image readout frame. If the time spent collecting the fixed pattern frames is required to be small compared to the integration time of the image frame, an upper limit is placed on n_{fp} implying a lower limit on the fixed pattern noise.

Fixed-patterned frames: these numerically generated frames are the difference between an image readout frame and an averaged fixed pattern frame. Using equation 1.3 to combine the noise of the two operand frames, the noise of a pixel in a fixed patterned image frame is found to be

$$\sigma_{irf-fp} = \sqrt{\sigma_r^2\left(1 + \frac{1}{n_{fp}}\right) + N_p + N_d} \tag{1.6}$$

and therefore the signal-to-noise ratio of the information from that pixel is given by

$$\frac{S}{N_{fpf}} = \frac{N_p}{\sqrt{\sigma_r^2\left[1 + \frac{1}{n_{fp}}\right] + N_p + N_d}} \tag{1.7}$$

Flat-fielded frames: these numerically generated frames are the quotient of a fixed-patterned image frame and a flat-field frame. The flat-field frame is a fixed-patterned frame whose image is of a spatially uniform illumination pattern, and the noise and signal-to-noise ratio of the individual pixels

within the operand frames are given by equations 1.6 and 1.7 respectively. The probability distribution of a fractional error will have the same functional form as the noise distribution of its signal. It follows that the distribution is Gaussian with a standard deviation equal to the quotient of the noise standard deviation and the signal, and that this standard deviation is the reciprocal of the signal-to-noise ratio of the signal. Thus the fractional uncertainty probability distribution of a quotient frame is the convolution of the operand distributions, and has a standard deviation found by using equation 1.3 of

$$\frac{\sigma_q}{S_q} = \sqrt{\left[\frac{\sigma_i}{S_i}\right]^2 + \left[\frac{\sigma_f}{S_f}\right]^2} \quad , \tag{1.8}$$

where i and f are the operands, and q refers to the quotient frame. The interpretation of equation 1.8 allows the signal-to-noise ratio of a flat-fielded frame to be found from the signal-to-noise ratios of the image and flat-field frames, respectively S/N_i and S/N_f, as

$$\frac{S}{N} = \left[\left[\frac{S}{N}\right]_i^{-2} + \left[\frac{S}{N}\right]_f^{-2}\right]^{-0.5} \tag{1.9}$$

Thus in the general case, the signal-to-noise ratio of the final image frame is seen to be degraded by the transfer function correction process. The noise of the image and flat-field readout frames, given by equation 1.4, are augmented by the subtraction of the averaged fixed-pattern frame, whose noise is given by equation 1.5. The signal-to-noise ratios of the resulting fixed-pattern frames are given by equation 1.7, and determine the signal-to-noise ratio of the flat-fielded frame according to equation 1.9. This result shows that the division by the flat-field further decreases the signal-to-noise ratio of the image. However the degradation of the available signal-to-noise ratio in the image read-out frame can be kept within any arbitrary limit if the number of fixed-patterns to be averaged is sufficiently high, and if the ratio $(S/N)_f/(S/N)_i$ is sufficiently large.

1.2.4 The Detector Noise Domains

If the dark signal generation rate in a detector is negligible compared with the signal photon detection rate, then equation 1.4 shows that there are two independent noise sources which contribute to the net detector output noise: the readout noise and the photon shot noise. Therefore the net noise of any one frame can be characterized as follows.

Readout noise limited domain: when the detected photon signal of a pixel is negligible by comparison to the square of the readout noise of the pixel, the signal is said to be readout noise limited. In this response domain the noise is independent of the signal level, and thus the signal-to-noise ratio is linearly dependent on the signal level.

Photon noise limited domain: when the square of the readout noise of the pixel is negligible by comparison to the detected photon signal in that pixel, the signal is said to be photon noise limited. In this response domain, both the noise and signal-to-noise ratio are equal to the square-root of the detected photon signal. An additional property of operating in this domain is that the subtraction of the fixed-pattern, in the transfer function correction process, does not contribute to the net output noise.

A detector whose operating principle is to count the individual photons that have been detected is classified as a photon counting detector. Those detectors will not exhibit readout noise and so will always operate within the photon noise limited domain. Detectors whose operating principle is to represent the total number of photons detected by each pixel as the magnitude of a physical parameter, are classified as integrating detectors. All current integrating detectors exhibit a readout noise which is greater than their representation of a single detected photon. Therefore at low signal levels they operate within the readout noise limited domain wheras at sufficiently high signal levels, they can operate within the photon noise limited domain.

1.3 Dynamic Range

The dyanamic range of a detector specifies the range of responses to which the detector can respond. Therefore quantifying dynamic range depends on how the response of the detector is defined. For this purpose, the response will be defined to be the response from a single pixel when measured in units of the signal level that corresponds to unit signal-to-noise ratio (but alternatively see Livingston et al. 1976). For a readout noise limited detector that exhibits a fixed-pattern signal, the dynamic range is therefore the quotient of the maximum possible fixed-patterned signal and the net noise of the detector, as given by

$$\text{Dynamic Range} = \frac{\text{Maximum fixed-pattern Signal Level}}{\text{Combined Readout and Dark Noise}} \quad (1.10)$$

In the general case, the dynamic range of a photon counting detector is also given by equation 1.10 because of the detector dark noise, although both the readout noise and fixed pattern noise will be zero. However from the original definition, the dynamic range of a photon counting detector in the absence of dark noise will be the maximum number of photons that it can record.

Thus, dynamic range will be thought of as the maximum possible response of the detector relative to the minimum response at which the presence of an optical signal can be detected.

1.4 Detector Efficiency

A detector system can be thought of as an instrument that records the information encoded in an illumination pattern that is incident upon it. The efficiency with which the detector collects that information can be quantified as the fraction of the incident information that can be recorded.

1.4.1 Signal-to-noise Efficiency

This author uses the signal-to-noise ratio to quantify the information content of an image, as introduced in section

1.2.1. Therefore the efficiency with which a detector collects an image is defined to be the fraction of the signal-to-noise ratio available in the integrated incident image, that has been recorded by the detector in that integration time. The author refers to this quantity as the Signal-to-Noise Efficiency, SNE, and expresses it as

$$SNE = \frac{\left[\frac{S}{N}\right]_{recorded}}{\left[\frac{S}{N}\right]_{incident}} \qquad (1.11)$$

The SNE will be functionally dependent on the efficiency of the underlying quantum detection process of the detector.

1.4.2 Responsive Quantum Efficiency

The efficiency with which the quantum detection process occurs within the detector can be quantified by the probability of an incident photon being recorded, called the responsive quantum efficiency, RQE. It follows that in equations 1.4, 1.6, and 1.7, the number of detected photons, N_p, is given in terms of the integration time, Δt, the incident photon arrival rate, N_i, and the RQE as

$$N_p = RQE\ N_i\ \Delta t\ . \qquad (1.12)$$

Therefore in the case of a noiseless detector, the SNE can be expressed in terms of the underlying quantum detection process as

$$SNE = \sqrt{\frac{N_p}{N_i \Delta t}} = \sqrt{RQE} \quad ; \quad \sigma_i = 0\ . \qquad (1.13)$$

1.4.3 Detective Quantum Efficiency

A detector parameter in common use is called the detective quantum efficiency, DQE, and is defined to be

$$DQE = \frac{\left[S/N_{recorded}\right]^2}{\left[S/N_{incident}\right]^2} \qquad (1.14)$$

Therefore the DQE of a detector is equivalent to the RQE that a noiseless detector would exhibit under identical operating

conditions. The DQE parameter allows the effective efficiency of the quantum detection process in different detectors to be compared, but does not directly express the efficiency of a detector at recording its incident information. The dependence of the SNE on the DQE is

$$SNE = \sqrt{DQE} \tag{1.15}$$

CHAPTER TWO

THE LINEAR DIODE ARRAY DETECTOR

Before a detector system can be designed and operated, an understanding of the response of its sensor component to its input signal, control signals, and environment must be established. Therefore a qualitative description of linear diode arrays will be developed in order to understand why the responses occur, and upon what they depend. Also, these arrays will be modelled so that the processing of the sensor signal by the detector system can be optimized by a quantitative analysis.

2.1 Electronic Response And Parameters

2.1.1 The p-n Junction

The interface between regions of n-type and p-type semi-conductor is called a p-n junction. During the formation of the junction, the concentration gradients of electrons and holes drive them across it in opposite directions. When a given type of charge carrier crosses the junction, it leaves behind an oppositely charged immobile ion. Thus immobile net charges accumulate near each side of the junction, negative in the p-side and positive in the n-side. This is called the 'depletion region', and its internal electric field opposes the diffusive transport of charge across the junction. The formation of the depletion region is complete when these two processes reach equilibrium.

The junction is said to be reverse biassed if a potential is applied across it with the same polarity as that of the depletion region. The applied potential appears almost entirely across the depletion region due to an increase in the electric field of the region. This is because the net charge stored on either side of the junction increases, which is achieved by removing additional electrons from the n-side of the junction, and holes from its p-side. The dependence of the net stored charge in the depletion region on the applied

reverse potential is called the depletion region capacitance.

2.1.2 The Integrating Photo-diode Sensor

The photo-diode light sensor is a reverse biased p-n junction. In 1960 a patent was issued to F.W. Reynolds at Bell Telephone Laboratories describing a characteristic of the p-n junction which became known as 'Charge Storage Operation'. The diodes are operated in charge storage mode by reverse biassing their junctions to a certain initial potential to store a preset charge on the depletion region capacitance. The capacitance then discharges during the specified integration time by two principle mechanisms.

1) The internal photo-electric effect : If the energy of an absorbed photon exceeds the silicon bandgap energy, an electron is raised from the valence energy band into the conduction energy band to form an electron-hole pair. If diffusion transports this pair to the depletion region within their lifetime, they will not recombine, but will discharge the depletion region capacitance by one electronic charge.

2) Thermal charge generation: the thermal fluctuations in the energy of valence band electrons can raise those electrons into the conduction band. The probability of this depends on the temperature of the semi-conductor and on the reverse potential of the depletion region. Each electron-hole pair which diffuses into the depletion region within its finite lifetime will discharge the capacitance of the depletion region by one electronic charge.

At the end of the integration, the amount of charge required to rebias the depletion region capacitance to its initial value is the measure of the accumulated photon signal and thermal dark current.

The energy from electron-hole pairs which recombine with the crystal lattice, and from absorbed photons whose energy is less than the bandgap energy, appears as a propagating mechanical lattice vibration known as a phonon.

2.1.3 Physical Organization and Operation

As shown in figure 2.1, arrays of photo-diodes can be

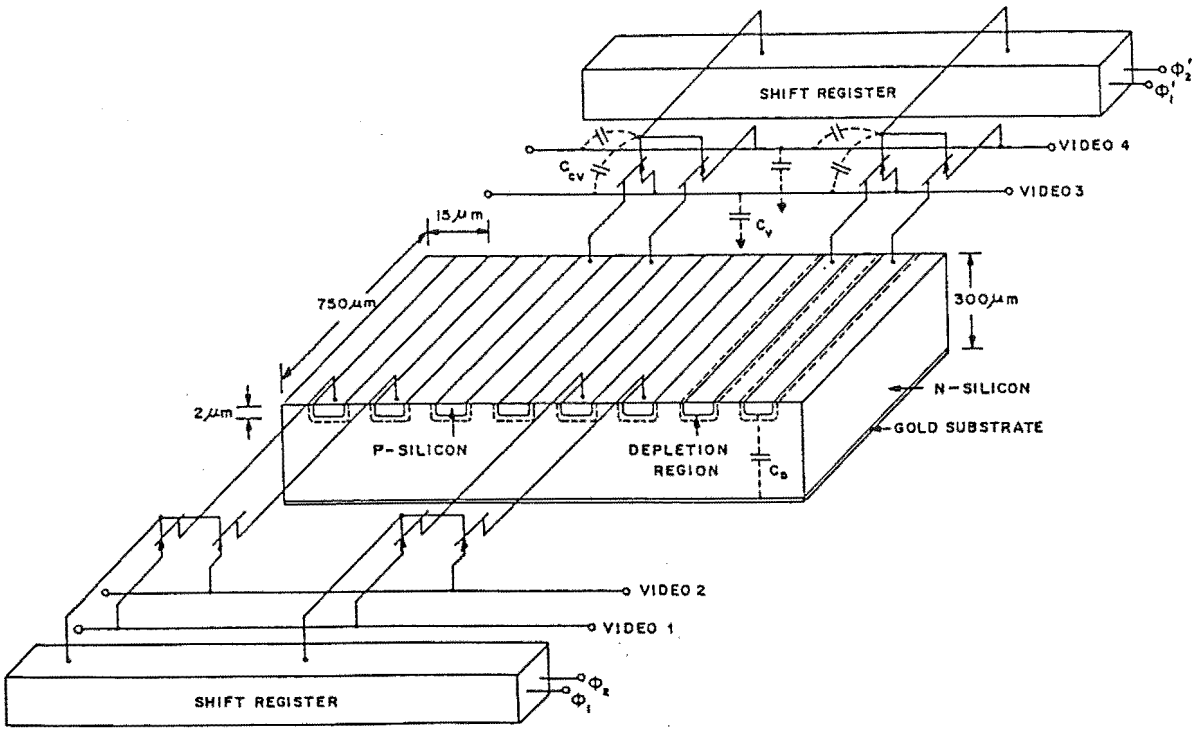


Figure 2.1: Schematic representation of the structure of the Reticon RLxxxxF/30 series photo-diode array. (based on Livingston et al. 1976)

fabricated by p-doping surface regions into an n-doped silicon substrate. The surface is coated with silicon dioxide to prevent surface leakage currents from contributing to the dark current, and to saturate the free lattice bonds as described in section 2.3.1. The height of the diode sensing area is delimited by a metal aperture encircling the array of diodes. Access to the diode signals is accomplished by two shift register scanning circuits that are fabricated on the same substrate as the array of diodes. For the RL936F/30 array, each circuit is composed of two video lines, an array of 234 pairs of MOSFET switches connecting the diodes to their appropriate video line, and a 234-bit shift register with three input control lines. Figure 2.2 shows a scheme of one of these circuits, which is of the generic type whose design has been described by Joynson et al. (1972). It operates when the time-varying voltage waveforms referred to as clocks, and shown in figure 2.3, are applied to the control lines. The voltages are either 'low' or 'high', and the transitions from low to high and high to low are respectively called rising and

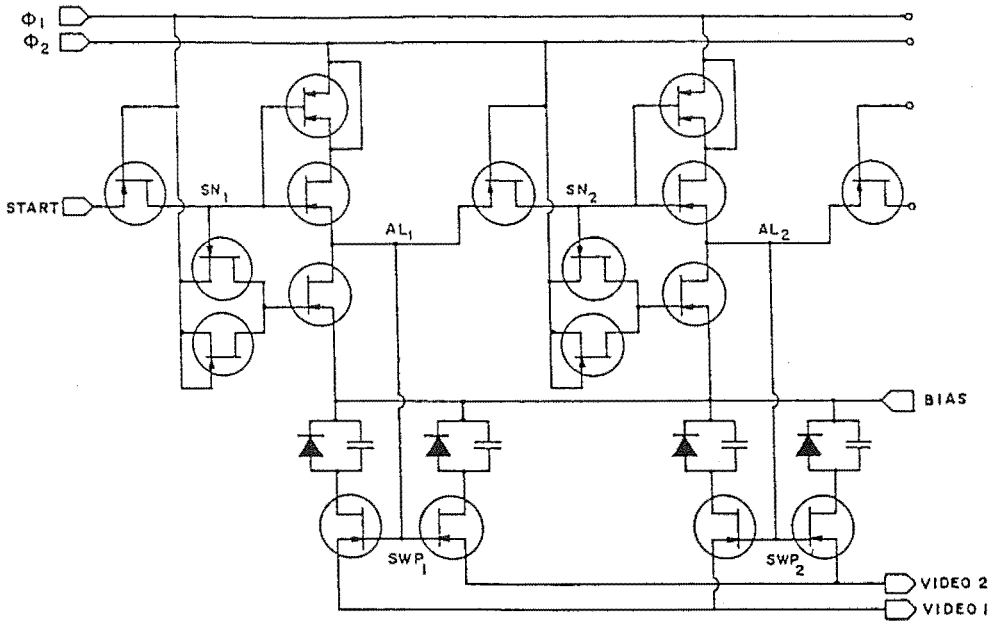


Figure 2.2: Circuit representation of a shift register (based on Joynson et al. 1972).

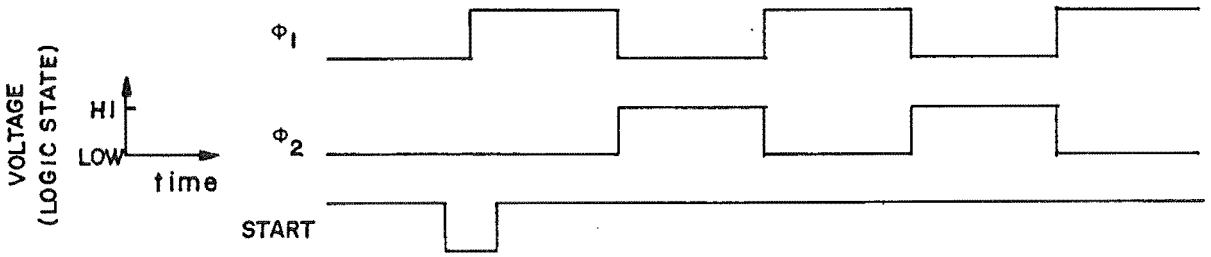


Figure 2.3: Time-varying waveforms (clocks, ϕ_1 and ϕ_2, and the start pulse) for the shift registers.

falling edges. Access to the diode array is accomplished when a charge packet referred to as a 'bit' is loaded into the shift registers first storage node, SN_1, by a rising edge of clock $\phi 1$ being cotemporal with a low start pulse. The falling edge of clock $\phi 2$ then shifts the start bit into the first address location, AL_1, thereby turning on the first pair of switches, SWP_1, in the multiplex switch array. That switch pair is subsequently turned off when the rising edge of $\phi 2$ moves the shift bit from address location one onto storage node two. The falling edge of $\phi 1$ then moves the shift bit into address location two to turn on the second switch pair, and later the rising edge of $\phi 1$ turns off switch pair two to end the first cycle of this control sequence. The cycle is repeated to sequentially access every pair of diodes addressed by the shift register. The two shift registers access

alternate pairs of diodes along the array.

2.1.4 The LDA circuit representation

The physical hardware of a video-line in a self-scanning photo-diode array has the equivalent electronic circuit representation shown in figure 2.4. The photo-diodes

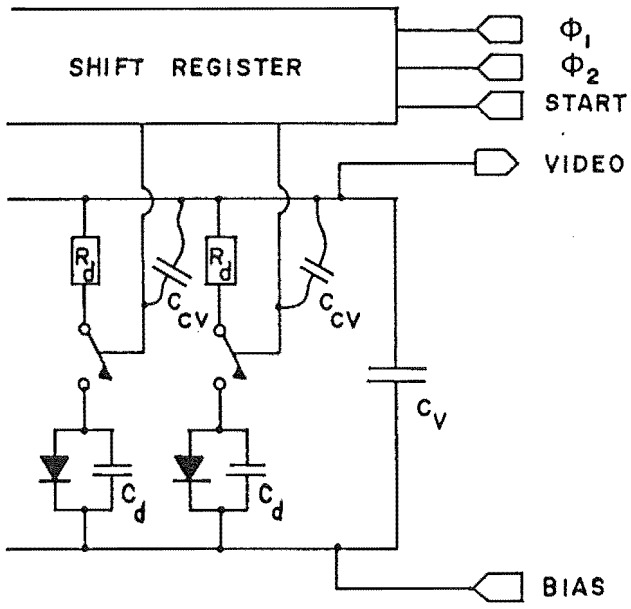


Figure 2.4: Equivalent electronic circuit for a self-scanning photo-diode array.

are represented by an ideal diode in parallel with their diode capacitance, C_d. The anode of each diode is connected to the video line through its own shift register addressed multiplex switch, with the 'on' resistance of the switch, R_d, explicitly shown. The cathode of each diode is connected to a common bias line to allow the diodes to be reversed biassed, and to reference the video line through 'on' diodes to the zero signal reference of the external electronics. Each multiplex switch exhibits a small ≈0.15 pF capacitance which effectively exists between the video and bias lines. Their parallel sum is represented as a single lumped component by the video capacitance, C_v. Additionally, each switch exhibits a capacitance between its control line and the video line which is represented by C_{cv}.

2.1.5 The Fixed Pattern

When a multiplex switch changes state, the transition in the clock voltage effecting the change will alter the potential across the capacitance C_{cv}. The quantity of charge required to change the potential of the capacitor must be sourced or sunk by the video line. Thus when a diode is selected by a falling edge during an array scan, and the previous diode is deselected by a rising edge, charge is both sourced and sunk by the video line. Imbalance in the C_{cv} capacitances between the two switches due to chip layout and fabrication differences will result in a net charge transfer between the two capacitors and the video line. The charge transferred is additive to the signal charge on the diode accessed by the video line, and is therefore a component of the fixed pattern of the diode array. Vogt, Tull, and Kelton (1978) have found that the amplitude of the fixed pattern charge is

$$q_{fp} = 500{,}000\ e^{-}/h \text{ pairs}. \qquad (2.1)$$

Wood (1979) has claimed that charge pumping in the MOSFET multiplex switches contributes the other major component of the fixed pattern. This mechanism removes charge from the conducting switch channel connected to the video line when the negative control pulse creates or annihilates the channel. This charge is pumped into the substrate of the switch, reducing the charge on the accessed diode in the additive manner of the fixed pattern.

Both the capacitance C_{cv} of the MOSFET switch gate to drain and gate to source capacitances, and the charge pumping mechanism, are temperature dependent. This requires operation of the diode array at constant temperature to stabilize the fixed pattern.

2.1.6 Intrinsic LDA Noise Sources

The diode access and reset phases of operating a self-scanning diode array generate intrinsic random fluctuations in the signal charge.

a) Thermodynamic Reset Noise

Charge must flow through a conductor or switch of non-zero resistance to reset the diode capacitance, and so the Johnson-Nyquist voltage noise of the resistance in that reset path (see appendix 2) will cause the reverse bias of the diode voltage to fluctuate during the reset time interval. The corresponding charge fluctuation on the diode capacitance is sampled at the end of the reset period, resulting in an uncertain initial charge on the reset diode. As the resistor noise voltage has an amplitude proportional to $\sqrt{R}$, and the noise bandwidth of the resistor-capacitor circuit is inversely proportional to $\sqrt{R}$, the reset noise amplitude does not depend on the resistance. Thus to calculate the noise amplitude, the fluctuation energy for a system with one degree of freedom, given by the equipartition theorem, is equated to the electrostatic energy fluctuation of the capacitor as

$$\frac{1}{2}\,kT = \frac{q_n^{\,2}}{2C_d} \quad ; \quad \left[= \frac{1}{2}\,C_d V^2 \right] \tag{2.2}$$

The r.m.s. noise in electronic charge units is then found to depend only on the absolute temperature T, and the diode capacitance as

$$q_n = \frac{1}{e}\sqrt{kTC_d} \tag{2.3}$$

Additionally, real MOSFET switches can have excess noise of up to $\sqrt{2}$ times their Johnson-Nyquist resistor noise, which will increase the thermodynamic noise by up to $\sqrt{2}$ (J.A.Hall 1976, p 554).

b) Fixed Pattern Noise

The transfer of charge through any potential barrier can be described with Poisson statistics, and the associated uncertainty in the net charge transferred is called shot noise. As the fixed pattern charge pumping transfers charge through the potential barrier between the conducting channel of the MOSFET switch, and the substrate, the quantity of charge removed from the video line exhibits shot noise.

c) Net Intrinsic Detector Noise

Two contributions of reset noise are made to any observation due to resetting the diode at both initialization, and readout. If a reset switch excess noise factor of F_x is used, and the net charge pumped is called q_p, the intrinsic detector noise is given by

$$\sigma_i = \sqrt{2F_x^2 \frac{kTC_d}{e^2} + q_p} \qquad (2.4)$$

If F_x = 1.2, T = 133 kelvins, C_d = 0.6pF, and $q_p \approx 8 \times 10^4$ e^-/h pairs (Wood, 1979), the intrinsic detector noise is calculated to be approximately 450 electron-hole pairs. However if F_x = 1 and q_p = 0 e^-/h pairs, then the lower limit on the intrinsic noise is approximately 290 e^-/h pairs.

2.2 Readout Techniques

The diode signal charge must be conditioned by an amplifier attached to the video line to enable subsequent signal processing to determine the integrated photon flux. This amplifier may be characterized as presenting either a high or a low impedance between the video line and the signal ground.

2.2.1 Video Voltage Level Processing

In figure 2.5 a high input impedance amplifier (see appendix 1) buffers the video line, and a low 'on' resistance reset switch interconnects the video and signal ground. As no charge can leak from the video line when buffered by this amplifier, any video line charge variation will appear as a voltage variation on the video capacitance.

a) Reset Switch Action

To reset the diode under access, the reset switch is activated to give the equivalent circuit shown in figure 2.6a. This action is the initialization for integrating incident

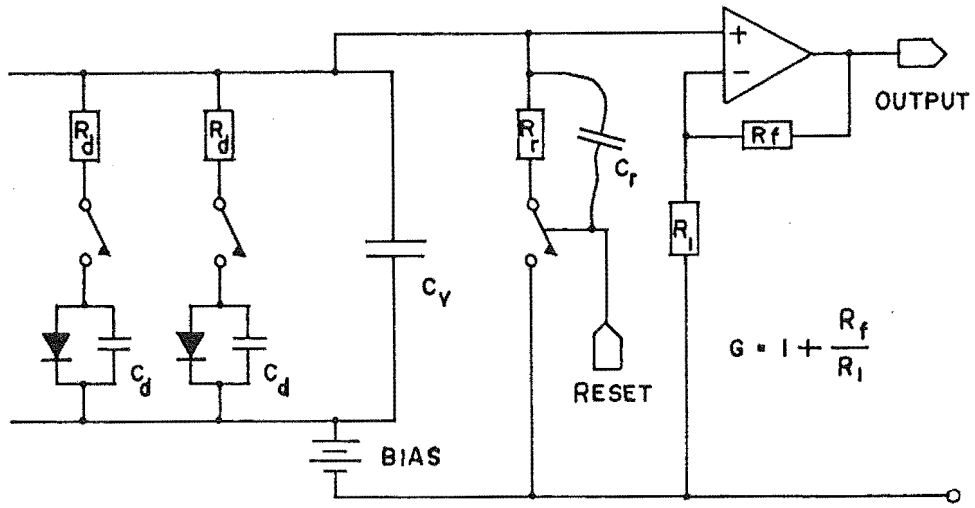


Figure 2.5: High input impedance amplifier conditioning the video signal.

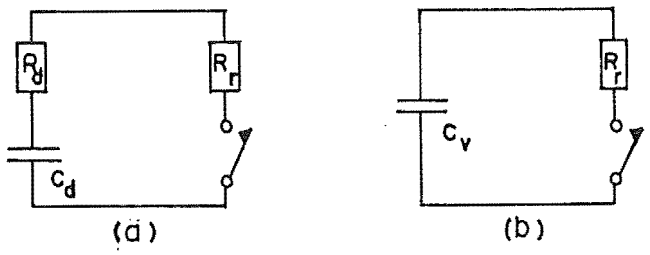


Figure 2.6: Equivalent circuits for initialization of
(a) diode capacitance, C_d, and
(b) video capacitance, C_v.

light referred to in section 2.1.2. The diode capacitance charges exponentially to the video bias voltage, V_b, with a time constant of $\tau_d = (R_d+R_r)C_d$, about 6 ns (Buss et al. 1976). The video capacitance is recharged in a similar way, as depicted in figure 2.6b, with a time constant of $\tau_v = R_r C_v$, about 400 ps. A reset period of N time constants will complete the recharging to one part in exp(N), and can be terminated when the residual charge is negligible compared to the detector noise.

At the end of the reset period the video voltage has settled to zero. This would be retained when an ideal reset switch was turned off because no charge would enter or exit the video capacitance. However the control voltage transition that turns off the reset switch will change the voltage across the undesirable capacitance C_r, requiring the video line to source charge into the capacitor. This reset feedthrough

offsets the video line voltage from zero to

$$V_r = \Delta V_{rp}\left[\frac{C_r}{C_r + C_v}\right] , \qquad (2.5)$$

where ΔV_{rp} is the amplitude of the reset control pulse. Since the charge is transfered through a capacitance, there is no shot noise associated with it. However the noise waveform on the reset control line will also feed through to the video line with the dependence of equation 2.5. Thus C_r must be minimized, and the reset control line noise must be kept to an appropriate value.

b) Readout Operation and Response

The integration is terminated by reading out the accumulated diode signal. Figure 2.7 shows the control signal

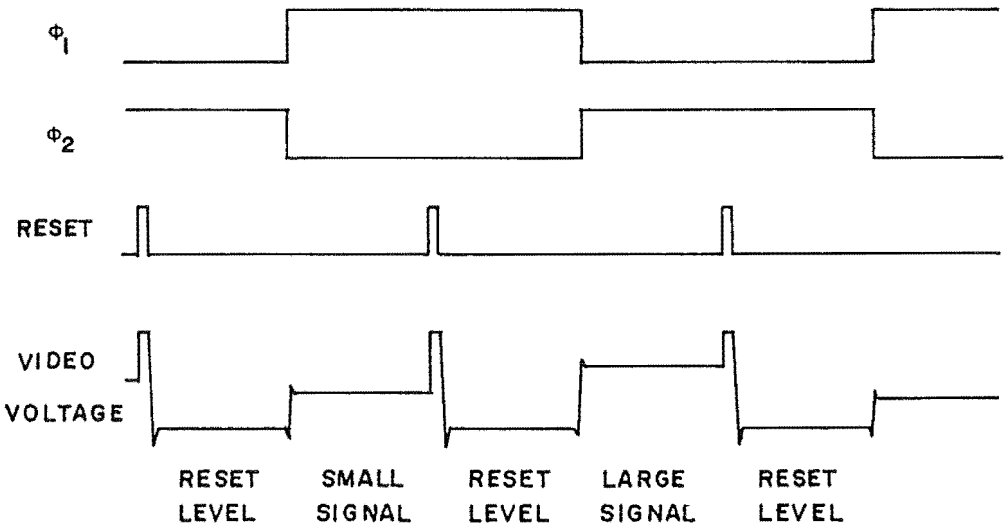


Figure 2.7: Schematic representation of the control signal timing, the reset switch action, and a typical video voltage output at readout.

timing and a typical video voltage response waveform of the readout. The diode that was accessed by the first falling edge of $\phi 1$ is reset during the middle of its access period; the video voltage is zero during reset, and exhibits the reset feedthrough offset immediately afterwards. This reset video voltage is held by the video line until the shift register action described in section 2.1.3 deselects this diode to

select the next diode. Fixed pattern charge is transferred onto the video line by this process as described in section 2.1.5; the video voltage changes in response to the charge. Also, the selection of the next diode allows the signal of that diode to be interrogated.

The voltages across the diode and video capacitances, as a function of the charge each holds immediately before the selection of the diode, are respectively given by

$$V_d = \frac{q_d}{C_d} \quad , \text{ and } V_r = \frac{q_v}{C_v} \; . \tag{2.6}$$

After selection, the diode charge, video charge, and fixed pattern charge appear on the parallel combination of the diode and video capacitances, changing the video signal voltage to

$$V_s = \left[\frac{q_v + q_d + q_{fp}}{C_v + C_d} \right] \; . \tag{2.7}$$

When the result $q_{fp} = V_{fp}(C_v + C_d)$ is used for the fixed pattern charge, the change in the video signal voltage due to the selection of the diode is

$$\Delta V_s = V_s - V_r = \left[\frac{C_d}{C_v + C_d} \right] \left[V_d - V_r \right] + V_{fp} \tag{2.8}$$

Since $V_d = V_r$ after resetting, the difference $V_d - V_r$ is the diode voltage change that has occurred due to the integration of the optically and thermally generated signal charge q_s. Therefore equation 2.8 can be expressed as

$$\Delta V_s = \left[\frac{\Delta q_s}{C_d + C_v} \right] + V_{fp} \tag{2.9}$$

which shows that the video difference voltage ΔV_s is linearly related to the signal charge, and has an additive fixed pattern component. Thus the quantity ΔV_s can be used by the subsequent signal processing to determine the photon signal.

The capacitance C_v in equation 2.9 is seen to attenuate the signal dV_s from its maximum possible value of $\Delta q_s/C_d$. As C_v is typically two orders of magnitude greater than C_d, the noise performance requirements of the readout electronics will be greatly increased. Therefore the existence of C_v is one of the significant problems of the self-scanning diode arrays.

c) Linearity

An implicit assumption of section 2.2.1b is that the depletion region capacitance of a p-n junction is linear; the charge stored is required to be linearly related to the reverse voltage. However the real dependence can be shown to be an inverse proportionality to the square root of the total junction voltage (Holt 1978, p42), and so equation 2.9 is non-linear. This would be an unacceptable signal extraction technique in the absence of the signal attenuation by the video capacitance. The attenuation restricts the signal voltage variations on these capacitors to be a very small fraction of their total reverse voltage. Since any continuous function appears linear to within some tolerance, if examined in a restricted range, the linearity of equation 2.9 in the region of operation is therefore greatly enhanced. Diode array signal extraction by this technique is found to be linear at the readout noise tolerance level (Vogt, 1981).

2.2.2 Recharge Current Processing

In figure 2.8 a low input impedance amplifier interfaces the video line to the external signal processing.

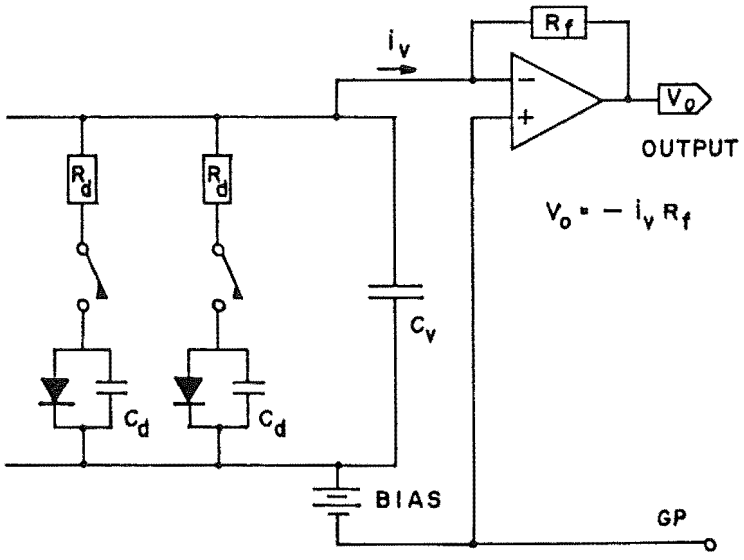


Figure 2.8: Low input impedance current-to-voltage amplifier interfacing a video line to the external signal processing.

Any charge on the video capacitance which would cause a deviation of the video voltage from zero, will flow into the amplifier until the video voltage has returned to zero. The amplifier represents this input current linearly as an output voltage.

a) Readout Operation

The integration is terminated by reading out the accumulated diode signal. Figure 2.9 shows the control signal

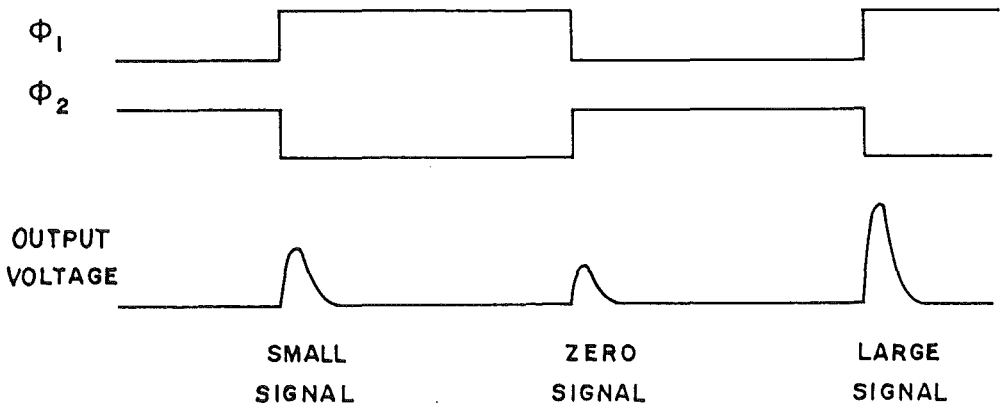


Figure 2.9: Schematic representation of the control signal timing for recharge current processing, and the resulting output signal.

timing and a typical video voltage response of a readout. The video voltage is zero when a diode is accessed by the next falling clock edge. The diode and video capacitance charges redistribute onto the parallel combination of those capacitances with a time constant of R_dC_d, and the fixed pattern charge is simultaneously transferred onto the video line. The video voltage would become that of equation 2.7, however the amplifier response is to supply a current pulse to restore the zero video voltage. The integral of that pulse is

$$\int_{pulse} i\, dt = q_s + q_{fp} \qquad (2.10)$$

and so the integral of the amplifier output in the ideal case is linearly related to the signal plus fixed pattern charge. Thus the recharge current pulse both resets the accessed diode

and measures the diode signal.

b) Performance and Stability

The recharge current pulse both starts and finishes with the same video voltage, so the non-linearity of the diode and video capacitances does not affect the total charge in the pulse. This signal extraction technique is therefore linear in the case of the ideal current to voltage amplifier of figure 2.9.

The infinite bandwidth of the ideal amplifier must be limited to reduce the amplifier noise to a finite level. In order to reproduce a pulse of fixed temporal width, the bandwidth must be such as to recover the pulse frequency spectrum $\sin(\pi f)/(\pi f)$ to the sixth zero crossing. An acceptably priced reproduction of a diode array recharge current pulse can be made with amplifiers which reach only the first zero crossing, a limit which includes most of the pulse energy. The consequence of this limitation is that the area of the output pulse has a dependence on the input pulse shape for a given input pulse area. Thus system instabilities which affect the pulse shape contribute directly to the readout noise. Since the fixed pattern charge pulse is the sum of the cotemporal charge pulses from the rising and falling clock edges, phase jitter between these two pulses results in the net charge pulse having an unstable shape. This instability can contribute significantly to the readout noise because the net fixed pattern pulse is typically larger than the signal pulse. Vogt, Tull, and Kelton (1978) have found that special attention to the stability of their clock waveforms is necessary, and Tull (1982) has needed additional clock electronics to negate a dependence of the clock phases on the temperature of the electronics. Wood (1979) chose to separate the clock edges in time, but finds that stringent requirements are then placed on the large signal handling capabilities of the amplifier because the full positive and negative amplitudes of the clock pulses must be handled separately.

2.2.3 Readout Technique Comparison

While recharge current pulse processing has been implemented in detector systems which have had a significant impact on astronomical research (Vogt, Tull, and Kelton 1978), alternatives should be considered in planning new systems. This author identifies the following considerations for choosing voltage level processing for diode array detectors.

1) The full diode capacitance energy is extracted by the voltage level processing technique, whereas for a comparable price, recharge current pulse processing does not because of its bandwidth limitation.

2) The voltage level processing technique produces a static signal which is stored on the video line enabling it to be integrated for sufficient time to reduce non-intrinsic noise sources to a negligible value. In contrast the current recharge pulse technique produces a dynamic signal whose short duration requires additional electronics to stretch the pulse before noise filtering and signal processing can be performed.

3) Current recharge pulse processing must explicitly handle the fixed pattern current pulse because it is simultaneous with the signal pulse. This leads to stringent stability requirements on the dynamic parameters influencing the fixed pattern. However an intrinsic property of voltage level processing is the integration of the fixed pattern and signal pulses on the video line storage capacitances. Therefore the processing of the video signal can be undertaken after the transient dynamic events of diode selection have finished.

4) The architecture for video level processing is now designed into the readout mechanism of charge coupled device detector chips, and so a diode array detector system using this technique will have a conceptual compatability with the premier astronomical detectors of today.

2.3 Performance Characteristics

2.3.1 Responsive Quantum Efficiency

The probability of a photon of wavelength λ being

recorded as a depletion region electron-hole pair in a photo-diode of temperature T is called the responsive quantum efficiency RQE(λ,T). Figure 2.10 shows RQE(λ) for a Reticon RL-1024S linear diode array operating at approximately 0 °C.

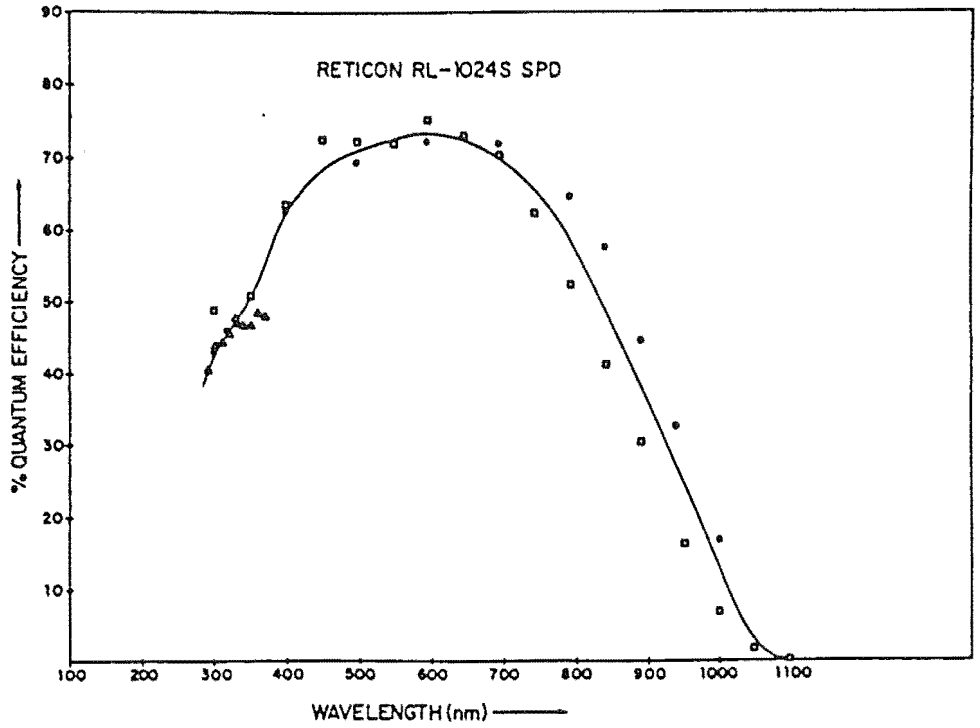


Figure 2.10: RQE for a Reticon RL1024S as a function of wavelength for T=0°C.
(adapted from Talmi and Simpson 1980)

To interpret the general characteristics of this curve, the following properties of silicon photo-diodes are used.

1) Only 70% of the light illuminating a silicon surface at normal incidence from a medium of air will pass into the silicon. This is because the reflectivity of that surface is

$$R_{sa} = \frac{\left[n_{si} - n_{air}\right]^2}{\left[n_{si} + n_{air}\right]^2} \qquad (2.11)$$

where n_{si} = 3.45 and n_{air} = 1.00, which are respectively the refractive indices of silicon and air.

2) The silicon optical absorption coefficient decreases with increasing wavelength, and consequently, the most probable depth of absorption moves from near the surface for short wavelengths, to deep within the silicon at longer wavelengths.

3) Not all photons are absorbed within the finite depth of

the semiconductor.

4) The depletion region layer has a finite depth and is below the surface of the silicon.

5) Some of the electron-hole pairs that are not created within the depletion region will recombine before they can be transported there. This is because the electric field in this region is weak due to most of the field associated with the reverse potential of the diode appearing across the lower conductivity depletion region. Thus the electron-hole pairs are only slowly transported to the depletion region which enhances their probability of recombining because they have finite lifetimes.

6) Some of the electron-hole pairs generated within the bulk of the silicon are not collected by the depletion region capacitance because they are captured in bulk traps. Those traps are the energy levels that occur in the band gap due to the presence of impurity ions and crystal defects.

7) Some of the electron-hole pairs generated near the silicon surface are not collected by the depletion region because they are captured in surface traps. Those traps are energy levels in the band gap of the surface silicon which are due to the unsaturated bonds at this discontinuity in the tetrahedral silicon lattice. The density of those traps is minimized by thermally oxidizing the surface to saturate the bonds by forming silicon dioxide.

By separating the RQE(λ) curve into three distinct wavelength regions, it can be qualitively interpreted.

250nm -450nm : the mean absorption depth is near the surface but their separation increases with increasing wavelength (#2 above). Therefore the losses due to surface trapping (#7) decrease with increasing wavelength, and so the RQE increases with wavelength.

450nm - 700nm : the mean absorption depth is passing through the depletion region in this wavelength interval (#2 and #4) and so the internal losses (#5, #6, and #7) are at a minimum. Therefore the RQE approaches the maximum value allowed by the surface reflectivity of silicon (#1).

700nm - 1100nm : the mean absorption depth is below the depletion region and their separation increases with increasing wavelength (#2). Therefore the RQE decreases with

increasing wavelength due to the increasing losses from bulk trapping and recombination (#5 and #6). The RQE becomes zero near 1100nm, the wavelength of photons whose energy is equal to the silicon bandgap energy.

Figure 2.11 shows the RQE temperature dependence by plotting RQE(T) / RQE(T=-30°C) against wavelength. At

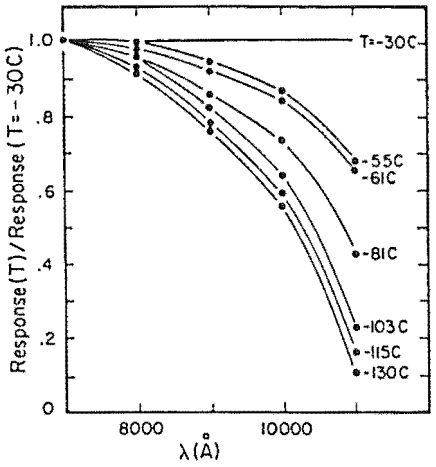


Figure 2.11: RQE as a function of temperature and wavelength. (from Vogt, Tull, and Kelton 1978)

wavelengths greater than 700nm, the RQE decreases with both decreasing temperature and increasing wavelength. This is due to the optical absorption coefficient decreasing with the same dependence, resulting in an increase in the separation between the depletion region and the mean absorption depth, and a consequential decrease in the RQE.

2.3.2 Modulation Transfer Function

If light of wavelength λ is imaged onto a detector in a spatially sinusoidal intensity pattern, of spatial frequency f and unit amplitude, the modulation transfer function MTF(f,λ) of that detector is the maximum peak to peak signal with which it can respond. Figure 2.12 gives curves of MTF(f=const.,λ) for frequencies corresponding to periods of 2p, 4p, and 8p, and an interpolated curve for 3p, where p is the width of one detector pixel. Also shown are the theoretical MTF values for the above frequencies which were found from equation 2.12 (see for example Barbe, 1976 p.665).

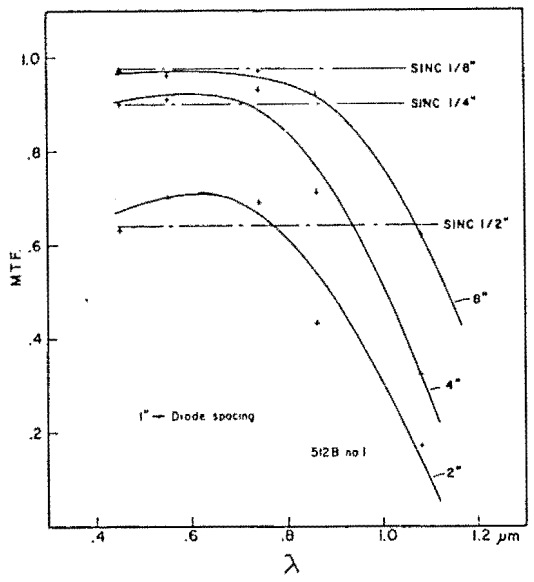


Figure 2.12: MTF as a function of wavelength for the sampling frequencies shown. (from Livingston et al. 1976)

$$MTF(f) = \frac{\sin\left[\frac{\pi}{2}\frac{f}{f_n}\right]}{\left[\frac{\pi}{2}\frac{f}{f_n}\right]} \qquad (2.12)$$

For wavelengths greater than 700nm, the MTF decreases with increasing wavelength as the separation between the mean absorption depth and the depletion region increases. This increasing separation allows increasing lateral motion as an electron-hole pair is transported up to the depletion region, enhancing the probability than a photon detected under one pixel will be recorded in an adjacent pixel. Consequently, the increased pixel width will decrease contrast, and therefore the MTF.

2.3.3 Thermal Leakage Current

The thermal leakage current is the time rate of thermal charge generation as described in section 2.1.2. For silicon photo-diodes, the temperature dependence of this leakage was found by Ghausi (1965) to be

$$I_t = (\text{const})T^{3/2}\exp(-7015/T) \quad cm^{-3}. \qquad (2.13)$$

The measured temperature dependence of thermal leakage for

three different linear diode arrays is given in figure 2.13. Campbell (1977) fits his data to equation 2.13 quite well. The data of Vogt (1981) deviates decisively from equation 2.13 for temperatures below -50°C, however he identifies faults in his experimental technique which could account for this. Fitting the data of Vogt, Tull, and Kelton (1978) to equation 2.13 is not useful because the same cooling configuration was not used for all the data points on their curve.

The detectors described in these last two papers are reported by Vogt (1981) to exhibit a temperature independent leakage current of up to several electron-hole pairs per pixel per second. Vogt, in consultation with others, reports a possible explanation for this as charge pumping by the continuously operated shift register clocks in their systems.

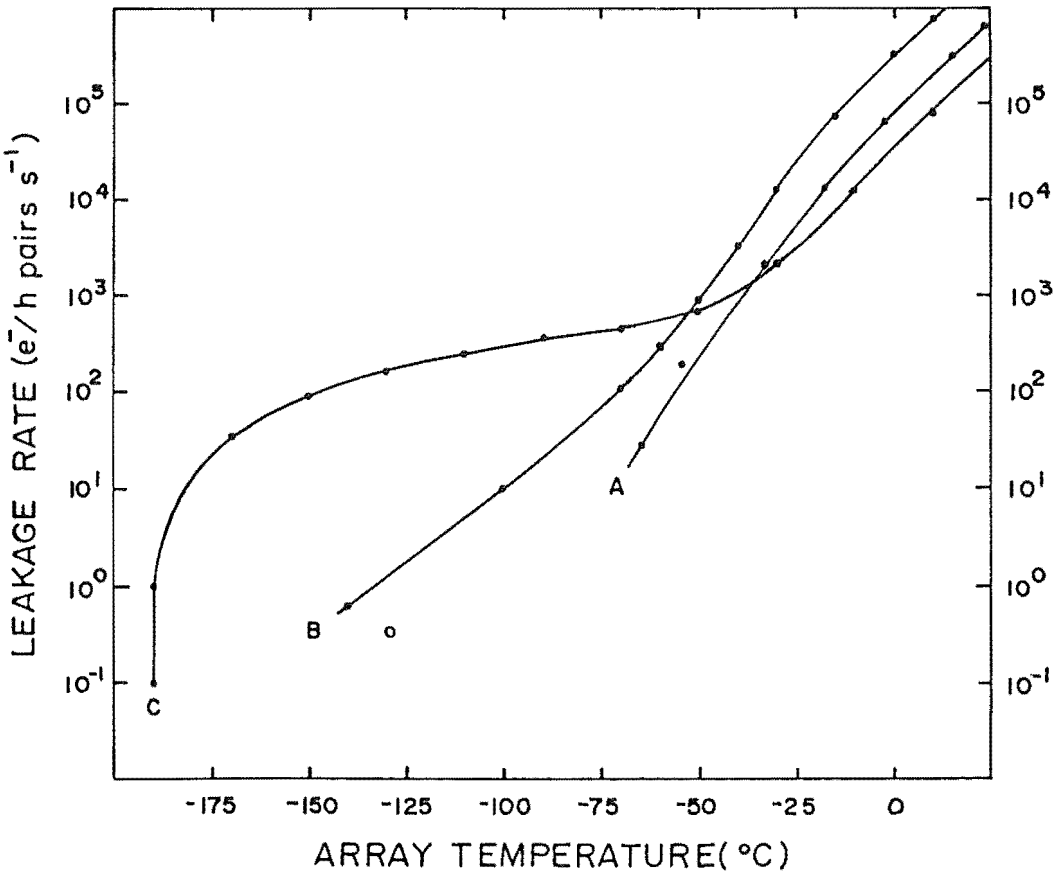


Figure 2.13: Thermal leakage versus temperature for different linear diode array systems

A: Campbell(1977)

B: Vogt, Tull, and Kelton(1978)

C: Vogt(1981)

The open circle represents the MJUO LDA system.

2.3.4 Blooming and Image Lag

Blooming, the loss of signal charge from a high signal pixel to an adjacent low signal pixel, could not be detected by Horlick (1976). However image lag, the retention of signal after the array has been readout and reset has been reported. Vogt, Tull, and Kelton (1978) measure a 1% lag for their system which uses the recharge current pulse readout technique. The feedback resistance of the amplifier in this technique forms a reset time constant with the video capacitance which can account for the existence of lag. Vogt (1981) finds no significant evidence of image lag in his system which uses video voltage level processing.

2.3.5 Cosmic Ray Sensitivity

The μ-meson component of the cosmic radiation can readily penetrate a typical detector enclosure, and so may pass through the detector with each particle creating an undesirable trail of up to 60,000 electron-hole pairs within a characteristic width of several pixels (Vogt, Tull, and Kelton 1978). For any specified meson energy, the mean quantity of charge in a trail is dependent upon the thickness of the diode array substrate, and therefore the thick 300μm substrate of Reticon arrays is a disadvantage. Analysis of cosmic ray events detected by CCD detectors show a majority of events occur in pairs and groups (Marcus, Nelson, and Lynds 1979), and therefore must be attributed to secondary radiation from interactions in the immediate environment of the detector.

More subtle effects arise from the illumination of the array by cosmic ray-induced Cerenkov light pulses originating in the quartz window of the array. The radiation is emitted into a cone of 48° vertex semi-angle centred about the cosmic ray's direction of motion, and will spread over several hundred diodes producing subtle changes in the continuum.

2.4 Operation Requirements

The preceding description of diode array sensors can be

used to establish guidelines for the design and operation of a linear diode array detector system. These guidelines are identified within the following subdivisions.

1) Environmental: the diode array must be operated isothermally to stabilize the on-chip capacitances which determine the fixed pattern and flat field responses. The temperature must be sufficiently low that the thermal leakage is fully tractable and does not cause non-linearity, but not so low that the near infra-red RQE is degraded more than is necessary. The sensor must either be operated in a vacuum, or in a gas free of contaminants that may freeze out onto the sensor at its operating temperature.

2) Shift-register clocks: the level transitions of different clock waveforms should not be cotemporal so that the fixed pattern charge contribution from the transition of one waveform is independent of the transition dynamics of the other waveform. The clock waveform amplitude instability and noise must be as low as is practicable so that their coupling to the video lines contribute significantly less than the intrinsic detector noise.

3) Signal processing: the intrinsic sensor noise should be the single dominant source of readout noise. The signal processing should be linear over the system dynamic range to within a peak-to-peak error equal to the net readout noise. The deleterious effect of the preamplifier input current on the stored video charge should be comparable to or less than the system readout noise during the diode access time. Drift in the diode rebiassing voltage supply should be sufficently low that the initialization and readout rebiassing of the diodes is the same to within the readout noise accuracy over all likely integration times.

4) Reset switch: the reset switch gate to drain capacitance must be the lowest that is obtainable to minimize the reset feedthrough video offset voltage, and the feedthrough of reset waveform noise. The switch leakage current should also meet the preamplifier input current specifications.

CHAPTER THREE

ELECTROMECHANICAL DESIGN

The physical design with which an electronic system is fabricated must allow the circuits to perform their required operational functions. The requirements of that design must be identified, the techniques for achieving them must be developed, and then the electromechanical design must be produced.

3.1 Electromagnetic Compatability

Electrical and electronic devices are said to be electromagnetically compatable when the electromagnetic noise generated by each cannot cause a malfunction or performance degradation in any of the others. Therefore the components within a subsystem, the subsytems within a system, and systems operating within a common electromagntic environment must all be electromagnetically compatable (EMC).

3.1.1 Electromagnetic Interference

The presence of currents or voltages originating from one device, the emitter, and causing a malfunction or performance degradation in another device, the susceptor, is called electromagnetic interference (EMI). The EMI emitter may be within the system of the susceptor, generating intra-system EMI, or it may be external, generating intersystem EMI. In all cases, EMI arises because of the simultaneous existence of three factors, at least one of which is not planned. They are a source of electromagnetic energy, a device sensitive to the type of energy being generated, and a transmission path for coupling the energy between them. The coupling taking place in any specified transmission path can be classified as one of two forms:

1) Conductive coupling: this form couples its energy through metallic conductors and through physical circuit components such as capacitors and transformers.

2) Radiative coupling: this form couples its energy through radiated electric and magnetic fields. The properties of the field are determined by the emitter, and by the media and separation between the emitter and susceptor. For separations less than $\lambda/2\pi$, where λ is the characteristic wavelength of the field, the properties of the field at the susceptor are primarily determined by the emitter: the susceptor is said to be in the near field, and the electric and magnetic fields are considered separately. At separations greater than $\lambda/2\pi$, the properties are primarily determined by the media: the susceptor is said to be in the far field, and the field is that of electromagnetic radiation.

The solution of Maxwell's equations for describing and quantifying EMI coupling in 'real world' configurations is impracticable. Therefore the coupling will be modelled by representing the physically distributed transmission paths with appropriate lumped components. Because the exact numerical values of these lumped components are difficult to determine for non-trivial geometries, this representation will give an approximation to the correct numerical answer. However, it will clearly show how the EMI coupling depends on the system parameters. Therefore general models will be examined for the most common forms of conductive coupling and near field radiative coupling, and this will allow guidelines to be established for minimizing the EMI.

a) Common-impedance Coupling

Every conductor used for transmitting signals from one position to another has a finite impedance composed of its resistance and inductance. When more than one circuit shares the same conductor, those circuits have that impedance as a common component. The influence of one circuit on another can be found from the analysis of figure 3.1. The emitter and susceptor circuits share the same ground plane as a current return path, and hence the ground impedance Z. Each of the emitter and susceptor circuits is also depicted with a signal voltage source, V, an equivalent impedance for the general circuit impedances, Z_g, and a load impedance Z_l. The EMI is that voltage, V_{emi}, which appears across the load of the

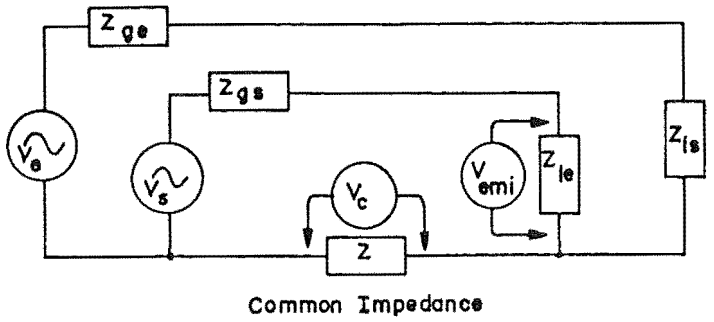


Figure 3.1: General circuit for common-impedance coupling.

susceptor circuit due to the operation of the emitter circuit. If we assume that the emitter circuit current is much greater than the susceptor circuit current, then the voltage across Z, which is common to both circuits, is

$$V_c \approx \left[\frac{Z}{Z_{ge} + Z_{le}}\right]V_e \quad \text{for} \quad Z << Z_{ge}+Z_{le} \ . \qquad (3.1)$$

The presence of that externally produced voltage in the susceptor circuit appears as the EMI voltage

$$V_{emi} \approx \left[\frac{Z_{ls}}{Z_{gs}+Z_{ls}}\right]V_c \quad \text{for } Z << Z_{gs}+Z_{ls} \ . \qquad (3.2)$$

Therefore substituting (3.2) into (3.1) explicitly gives the EMI voltage

$$V_{emi} = \left[\frac{Z\ Z_{ls}}{\left[Z_{ge}+Z_{le}\right]\left[Z_{gs}+Z_{ls}\right]}\right]V_e \ . \qquad (3.3)$$

The dependence of the EMI voltage on the common impedance should be noted because the typical source of that impedance is a conductor, in which both the inductance and resistive 'skin effect' will increase the impedance with frequency. This is significant to the electromechanical design of systems using high speed solid-state logic devices because of the following responses which occur when those devices make a logic state transition.

1) The amplitide of the current that the logic device is either sourcing to, or sinking from a static load will typically change when the logic state changes. This will require the power supply and/or ground conductor current to change by Δi within the transition time Δt of the output, and

will therefore induce a voltage pulse across the inductance L of that conductor with an amplitude of $\approx L\Delta i/\Delta t$. As depicted in figure 3.2, other voltage pulses will also be generated by the same mechanism during the transition time. They are due to the change in output voltage, ΔV, charging or discharging the output load capacitance, $C = C_s + C_i$, with a current pulse of amplitude $i \approx C\Delta V/\Delta t$. That pulse must return to the load through either the power supply or ground conductor, and so both the rise and fall of that pulse will induce voltage pulses across the inductance of the conductor. Therefore the signals of other circuits sharing the conductor will be corrupted by those pulses due to it coupling through the common circuit impedance.

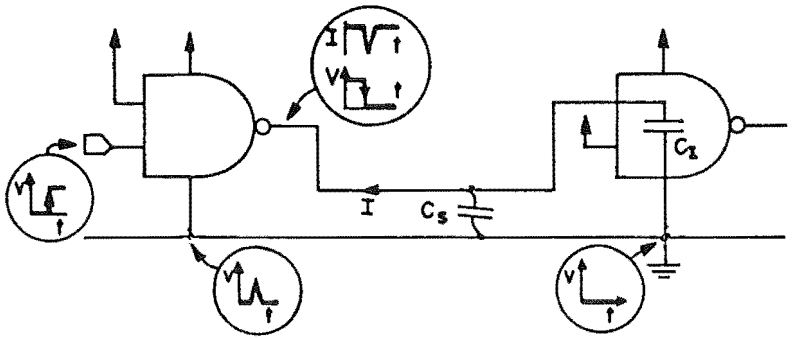


Figure 3.2: An example of an emitter-type logic circuit producing common-impedance coupling.

2) The push-pull circuit depicted in figure 3.3 is used as the output stage in the common families of logic devices, and is intended to have only one transistor switch closed at a time so that the output potential is either that of the power

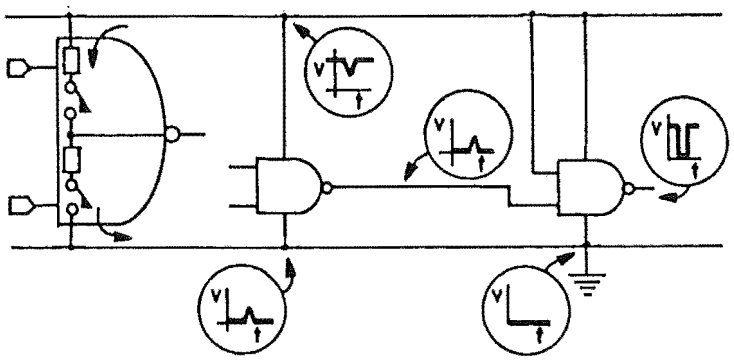


Figure 3.3: An example of a susceptor-type logic circuit producing common-impedance coupling.

supply or the ground. However, during the transition time required for the output to change from one state to the other, both transistors are on, allowing a current to flow from the power supply to ground which is only limited by the 'on' resistances of the transistors. Like the charging pulse for a load capacitance, this current pulse can cause common impedance coupling to any other devices on the same power supply or ground lines.

The principles of common impedance coupling will be applied to the specific situations of

1) grounding and shielding in section 3.1.2,

2) power supply distribution in section 3.1.3,

3) low level analogue signal transmission in section 5.3.2c3,

and 4) high speed logic circuitry in section 3.2.4a.

b) Electric-field Coupling

Electric field coupling occurs in the near field when a stray capacitance exists between the emitter and susceptor circuits. The EMI that occurs can be found from the analysis of figure 3.4. It is assumed that the impedance of the emitter node to ground is negligible compared to the impedance, Z_c, of the coupling capacitance C_c, which makes the emitter node appear as a voltage source to the circuit comprising the coupling impedance and susceptor circuit.

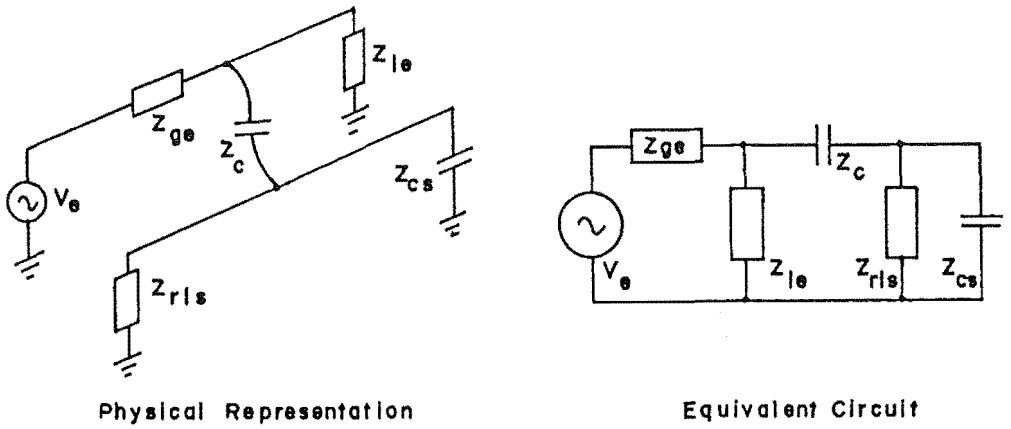


Figure 3.4: General circuit for electric-field coupling.
(a) The physical representation, and
(b) its equivalent circuit.

Therefore the EMI voltage is

$$V_{emi} \approx V_e \left[\frac{Z_s}{Z_c+Z_s}\right]\left[\frac{Z_{le}}{Z_{ge}+Z_{le}}\right] \quad \text{for } Z_{ge}//Z_{le} << Z_c \qquad (3.4)$$

where the second term is the voltage on the emitter node, the first term is the fraction of that voltage which appears between the susceptor node and ground, and Z_s is the impedance of the susceptor node to ground. The electric-field coupling configurations of significance to this work have $Z_{ge} << Z_{le}$, and can be classified as either the low or high frequency cases depicted by figure 3.5. These classifications are

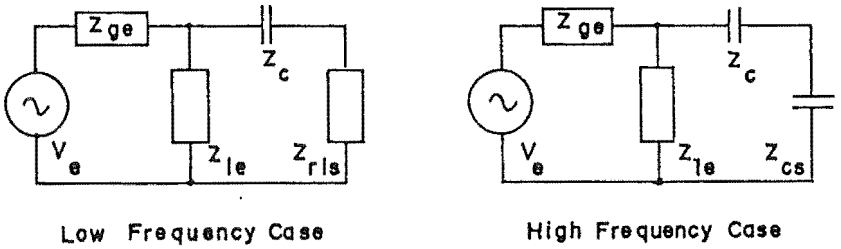


Figure 3.5: Electric-field coupling configurations in the (a) low, and (b) high frequency limit.

respectively defined by whether the net resistive and inductive impedance, Z_{rls}, of the susceptor node to ground is higher or lower than the capacitive impedance, Z_{cs}, of the susceptor node to ground. The EMI voltages for each case are respectively

$$V_{emi} \approx \omega Z_{rls} C_c \quad \text{for } Z_{rls} >> Z_c \,, \qquad (3.5)$$

and

$$V_{emi} \approx C_c/(C_c+C_s) \quad \text{for } Z_{rls} << Z_c \,. \qquad (3.6)$$

It follows that to reduce electric-field coupling, the coupling capacitance must be minimized, and the susceptor circuit impedance levels, Z_{rls} and Z_{cs}, must have the minimum value allowed for performing their required functions. C_c can be controlled by reducing the length of the conductors which are coupling, and by increasing their separation.

The principles of electric-field coupling will be applied to the specific situations of

1) grounding and shielding in section 3.1.2,

and 2) logic coupling to the video line in section 5.3.2c3.

c) Magnetic-field Coupling

Consider an electronic configuration whose physical representation and equivalent circuit are depicted by figure 3.6. Magnetic-field coupling occurs through the near field

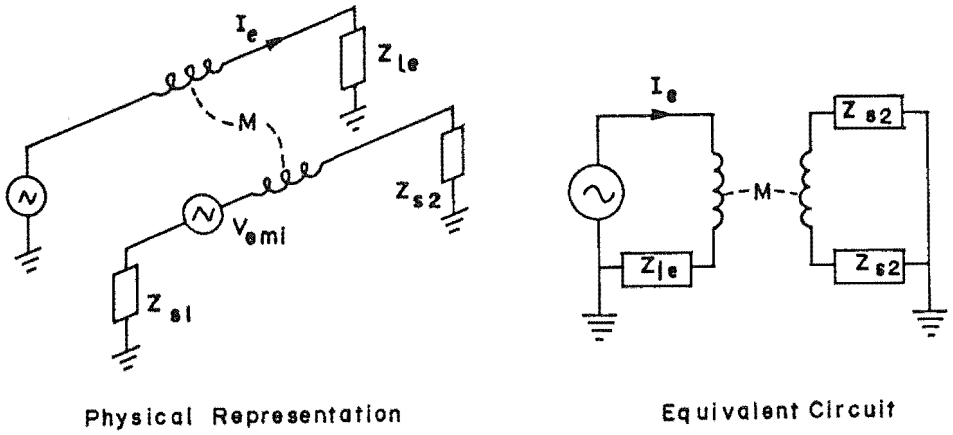


Figure 3.6: General circuit for magnetic-field coupling.
(a) The physical representation, and
(b) its equivalent circuit.

when an emitter circuit current, I_e, produces a magnetic flux, Φ_{es}, in a susceptor circuit which is proportional to that current and due to a stray mutual inductance of

$$M_{es} = \frac{\Phi_{es}}{I_e} \quad . \tag{3.7}$$

Therefore using Faraday's law, the emitter circuit current can induce an EMI voltage into the susceptor circuit of

$$V_{emi} = - \frac{d\Phi}{dt} = - M \frac{dI_e}{dt} \quad . \tag{3.8}$$

The emitter circuit current has the general time dependence of

$$I_e(t) = \int_o^\infty I_e(\omega', t)d\omega' = \int_o^\infty I_e(\omega')e^{i\omega t}d\omega' \tag{3.9}$$

and without loss of generality, the EMI voltage of a single frequency component, $\omega' = \omega$, can be found using equation 3.8 as

$$V_{emi} = -j\omega M I_e(\omega) \quad . \tag{3.10}$$

A typical coupling configuration is depicted by figure 3.7, for which the mutual inductance, and therefore the EMI voltage, can be found in terms of the physical circuit

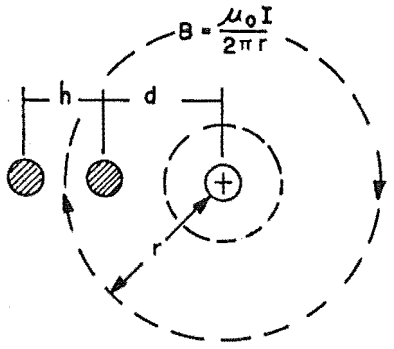


Figure 3.7: A simple, but important example of magnetic-field coupling.

parameters. One conductor in this emitter circuit is assumed to produce all the coupling flux, and it runs parallel to and in the same plane as the susceptor circuit, whose length is ℓ. Ampere's law gives the flux density at a radial distance r from the emitter wire, which when integrated over the area of the susceptor circuit, gives the coupling flux as

$$\Phi_{es} = \int_{d}^{d+h} BdA = \int_{d}^{d+h} \frac{\mu I}{2\pi r}\, \ell dr = \frac{\mu \ell I}{2\pi} \ln\left[\frac{d+h}{d}\right] . \qquad (3.11)$$

Therefore the EMI voltage induced into the susceptor circuit is found using equation 3.8 as

$$V_{emi} = - \mu \ell \omega I_e(\omega) \ln\left[\frac{d+h}{d}\right] , \qquad (3.12)$$

and it appears in series within the susceptor circuit. This is in contrast with an EMI voltage due to electric-field coupling which appears in parallel with the susceptor load.

It can be seen from equation 3.12 that to minimize magnetic- field coupling, the following circuit parameters must be set as close to the indicated extreme as is consistent with the required circuit functions.

1) Minimize the loop area of the susceptor circuit,

2) orientate the emitter and susceptor circuits to minimize the susceptor circuit loop area as seen by the emitter circuit,

3) maximize the separation of the emitter and susceptor circuits,

4) maximize the impedance of the emitter circuit,

and 5) minimize (filter) the bandwidth in the emitter circuit.

The principles of magnetic-field coupling will be applied to the specific situations of

1) power supply and signal distribution in section 3.3.2, and 2) printed circuit board design in section 3.2.4a.

d) Methods of Controlling EMI

In all but the simplest cases, a single unique solution may not exist for reducing EMI to an acceptable level. The primary techniques which can be applied to control EMI may be categorized into one, or more, of the following divisions

1) grounding,
2) shielding,
3) isolation,
4) balancing,
5) separation and orientation,
6) circuit impedance level control,
7) filtering,
8) cancellation techniques (frequency or time domain), and 9) cable design.

Discussions of these techniques, and their implementation, can be found in Ott (1976) and White (1973), which includes a detailed discussion of EMC. Of these techniques, grounding and shielding are the foundation of all non-trivial electro-mechanical designs, and will be examined at the circuit and system level in the following section. An outstanding discussion of these is given by Morrison (1967).

3.1.2 Grounding and Shielding

The term ground is used to refer to any point or distribution of points within an electronic complex whose potential is intended to be that of the zero-signal level. It is typically a conductor that distributes the zero-signal reference to the components of a complex, and is said to be earthed if it is ohmically connected to the local earth potential. Grounding and earthing are not synonyms.

A shield is a conductive partition placed between two regions of space to control the propagation of electric and magnetic fields between the regions. Shields may be applied

to keep electromagnetic radiation out of a region containing circuitry susceptible to it, or to contain the radiation of an emitter.

a) Signal Sources, Amplifiers, and Grounding

Each signal source in this work can be represented as a two-terminal series network; one terminal defines the zero-signal potential, and the network elements are a signal voltage source, V_s, and a signal source impedance, Z_s. The signal from each source will be conditioned by one of the two categories of amplifiers, which are defined as follows.

1) Single-ended amplifiers: the single-ended amplifier depicted in figure 3.8 will amplify the signal V_s, developed relative to the amplifier zero-signal reference, and present it in conditioned form relative to that same zero-signal reference. The amplification factor is called the single-ended gain, A_{se}.

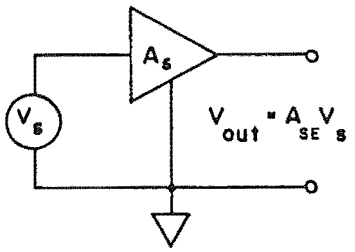


Figure 3.8: A single-ended amplifier.

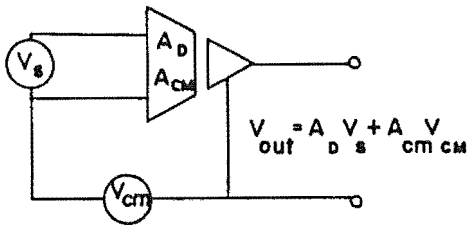


Figure 3.9: A differential amplifier.

2) Differential amplifiers: the differential amplifier depicted in figure 3.9 will amplify the signal V_s developed relative to one zero-signal reference, and present it in conditioned form relative to a second zero-signal reference. In general, the voltage between the two zero-signal references will be a non-zero function of frequency, and is called the common-mode voltage, V_{cm}. It follows that the common-mode gain, A_{cm}, is required to be zero so that the output signal is purely the product of the input signal and the differential gain. However consider a source and differential amplifier as depicted in figure 3.10a,b. The difference in impedance of

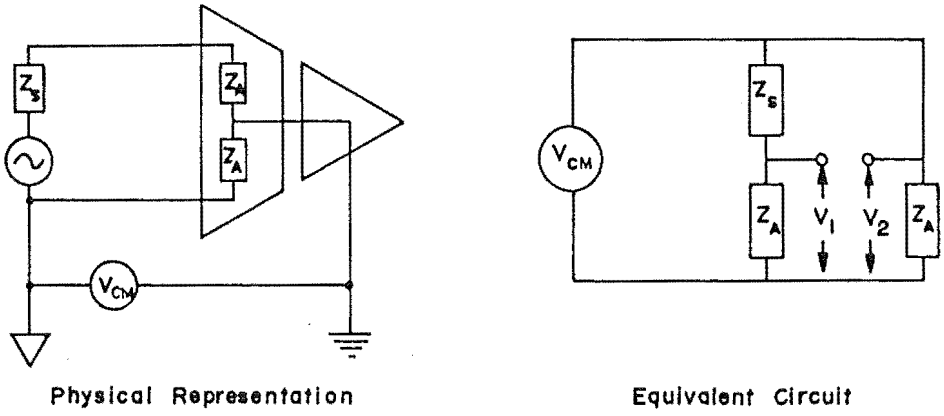


Figure 3.10: The (a) physical representation, and (b) equivalent circuit for determining the EMI of a differential amplifier with a source impedance imbalance (from Ott 1976).

the source terminals relative to the source ground is called the source imbalance. It can be seen that the combination of a source imbalance and common-mode voltage will form an undesirable differential input voltage of

$$V_{emi} = V_1 - V_2 = \left[\frac{Z_I}{Z_I+Z_s} - 1\right]V_{cm} . \qquad (3.13)$$

Thus even if the amplifier common-mode gain is zero, the presence of a source imbalance will cause a net non-zero common-mode gain for the source-amplifier combination. It can also be seen that the amplifier input impedance, Z_I, must be as high as possible.

It follows that the criteria for selection of each amplifier class are specified in terms of the connections between the source and amplifier grounds. They are:

1) Single-ended amplifiers: this amplifier type can be used if only a single connection must be made between the ground of the source and amplifier, and the ground of other circuitry. That point of connection is called the single ground point of the source and amplifier circuitry. However consider figure 3.11 which shows the physical representation and corresponding equivalent circuit for a source and single-ended amplifier circuit with two connections to external grounds. This shows that violating the single ground point criteria allows a common-mode potential to appear as an EMI

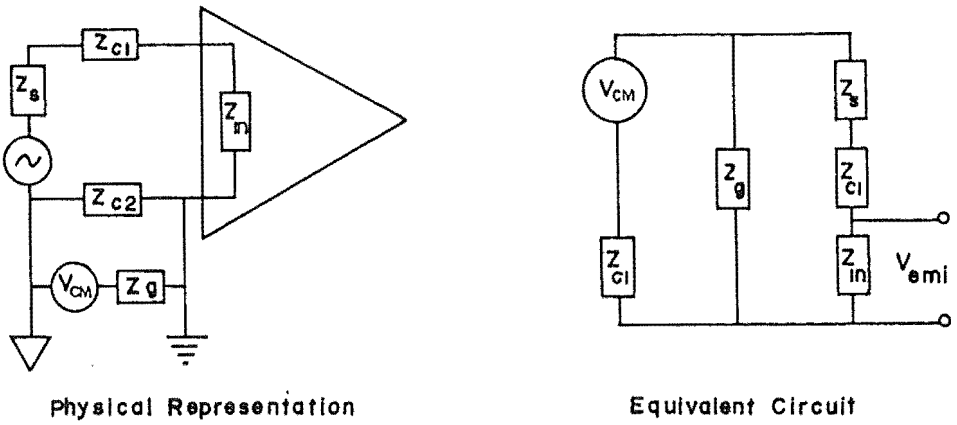


Figure 3.11: The (a) physical representation, and (b) equivalent circuit of a source and single-ended amplifier with an undesirable connection to the external ground (from Ott 1976).

amplifier input voltage of

$$V_{emi} = \left[\frac{Z_{in}}{Z_{in}+Z_s+Z_{c1}}\right]\left[\frac{Z_{c2}}{Z_{c2}+Z_g}\right]V_{cm} \qquad (3.14)$$

$$\text{for} \qquad Z_g // Z_{c2} \ll (Z_{in}+Z_s+Z_{c1}) \ .$$

2) Differential amplifiers: this amplifier type is used when i) the source and amplifier must operate relative to different ground references, which includes the special case of source and amplifier grounds being ohmically disconnected, and ii) when both signal source output terminals exhibit a high impedance to the signal source ground (see section b).

b) The Electrostatic Shield

A shield for the control of near field electic coupling is called an electrostatic shield, and is a fundamental component of non-trivial electromechanical designs. To apply such a shield to the current work, the appropriate principles of their application and operation must be developed in a similar way to Morrison (1967). Therefore consider figures 3.12a,b which are respectively the physical representation and equivalent circuit of an amplifier and source enclosed within a shield, and with an acceptable single connection to an

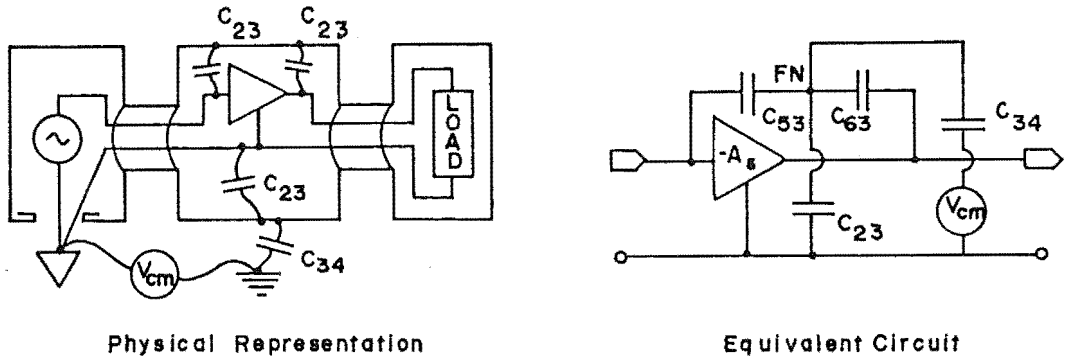


Figure 3.12: The (a) physical representation, and (b) equivalent circuit of an amplifier shield not connected to the electrostatically shielded circuitry (adapted from Morrison 1967).

external ground. As shown, unavoidable stray capacitances exist within the system which mix the common-mode potential into the signal. Even in the absence of the connection to an external ground, and therefore the components V_{cm} and C_{34}, an undesirable feedback network exists around the amplifier through the components C_{23}, C_{53}, and C_{63}. By connecting the system ground to the shield, the feedback node, FN, is shorted to ground which removes both these networks. Figure 3.12b depicts this, and shows that the only result will be an enhancement of the amplifier input and output capacitance. Therefore the following rule can be stated.

Rule 1: To be effective, an electrostatic shield should be connected to the ground of the circuitry it encloses.

The position for that connection can be found by considering the coupling of external ground potentials into the configurations shown in figures 3.13a and b. The stray capacitance between their shields and external grounds allows the ground potential to drive currents in the respective loops of 1-3-4-1 and 1-2-3-4-1. For non-zero emitter frequencies, these loops are also susceptor circuits for near-field magnetic coupling, and can therefore contain an additional current due to this mechanism. In figure 3.13a, this path is entirely external to the signal lines and it therefore will

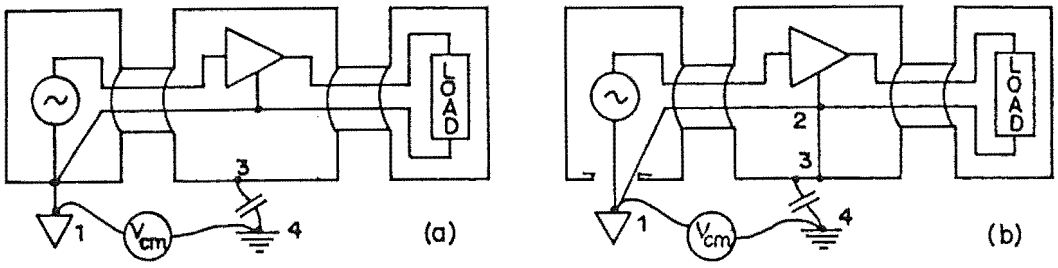


Figure 3.13: Two physical representations showing possible connections of the electrostatic shield to the signal ground (adapted from Morrison 1967).

not interact with them. However in figure 3.13b, the current passes through the signal ground line, and therefore its impedance, to generate an EMI voltage for the amplifier by common impedance coupling. Therefore a second rule can be stated which ensures that these EMI currents can exist only within the shield conductor.

Rule 2: If the signal ground is connected to an external ground, the connection of the shield to the signal ground must be at that same point.

The preceding system configurations conform to the grounding requirements of a single-ended amplifier because the load does not require connection to a particular external ground. This is the case of the signal being processed for either an internal system use, or for an external use if the load produces an optical signal which leaves the system.

When both source and load are connected to external grounds, the electronics within the two ground systems are interfaced with a differential amplifier as depicted in figure 3.14. The subsystems on either side of the differential amplifier can individually be considered as single-ended systems, and so they each have a shield governed by the preceding shielding rules. These shields are not connected at the differential amplifier to decouple stray capacitances like C_{23} and C_{24}. If this was not the case, those capacitances would degrade the theoretically infinite input impedance of the amplifier, and also allow the potential difference between

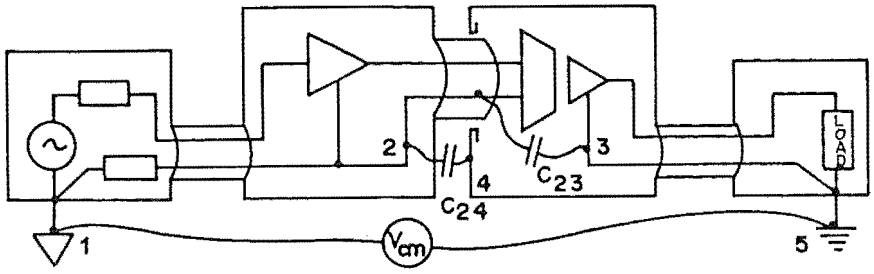


Figure 3.14: The physical representation of a correctly applied electrostatic shield to a differential amplifier (adapted from Morrison 1967).

the external grounds to drive currents through loops like 1-2-4-5-1 and 1-2-3-5-1. As previously found, both those properties would generate EMI.

c) The Utility Power Entrance

The instruments described in the previous sections require operating power, and the utility power is usually preferred over such alternative sources as batteries and solar cells, which can be internal to the system. Thus the utility power must enter the system through the electrostatic shield, and this can be effected by the transformer action used to convert the utility voltage amplitude to the required level. This is possible because the electrostatic shield is usually a non-magnetic material, and will allow a magnetic field to couple energy from a transformer primary coil outside the shield, to a secondary coil inside the shield. The shield or shields separating the coils can be an integral part of a transformer, and if connected to the system shield, form the required extension of that shield. Their design and implementation in a real transformer will be discussed in section 3.3.1b, but the requirements for their application to a system must initially be determined.

Therefore consider figure 3.15 which depicts a coil of n turns with one terminal connected to an electrostatic shield, and to ground, and with the average turn having a capacitance c_t, and therefore reactance X_c, to the shield. If the coil voltage is V, the voltage on the m th turn is V_m/n,

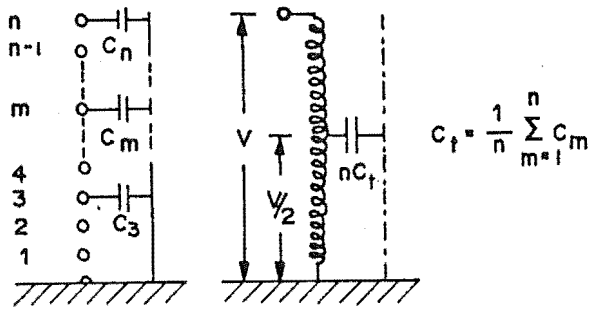


Figure 3.15: A coil depicted as a capacitance connected to the grounded, electrostatic shield (dash-dot line) (adapted from Morrison 1967).

and so the current in the capacitor coupling that turn to the shield is $V_m/n * 1/X_c$. So if n is large, the sum of the currents from all the turns to the shield is

$$I = \sum_{m=1}^{n} V\frac{m}{n}\,\frac{1}{X_c} \approx \frac{Vn}{2X_c} \qquad (3.15)$$

Thus the coupling of the coil voltage to a shield can be modelled as the total coupling capacitance combined into one component and connected to the turn which is at half the total coil voltage. Figure 3.16a shows these capacitances for the primary and secondary coil of a single shielded transformer. The primary coil current loop of 5-3-1-6-5 does not include a signal conductor, whereas the secondary coil loop of 7-3-1-2-7 will produce commom-impedance coupling in the signal ground.

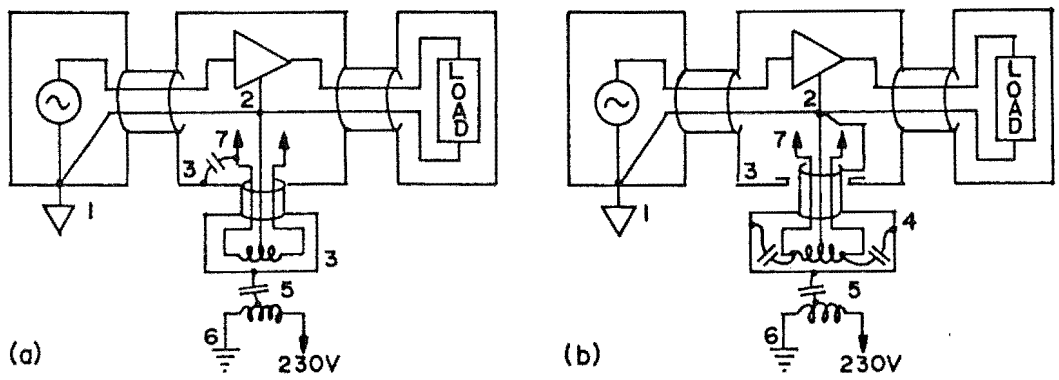


Figure 3.16: The two examples of ground-shield connections for a single-shielded transformer (adapted from Morrison 1967).

Figure 3.16b shows that the other choice of connection cannot eliminate coupling from at least one of the coils, and so the connection shown is preferred as the coupling comes from the lower voltage coil. In some applications the coupling is below an acceptable limit or can be filtered out, but in general a second shield must be introduced to the transformer as shown in figure 3.17. The coupling from the primary coil is now contained within loop 5-8-6-5 and the secondary coupling is similarly contained within loop 7-4-2-7. However coupling through the intershield capacitance allows common-impedance coupling in the signal ground due to the ground potential driving current through the loop 1-2-4-8-6-1. In some configurations this can be eliminated by returning the primary shield to the system shield and signal ground connection point. If the level of this coupling is still unacceptable, due possibly to a large ground impedance found in some signal sources, a third shield must be introduced to the transformer as shown in figure 3.18. The primary and secondary shields operate as in the case of the double shielded transfomer, and the third shield carries the current driven by the ground potential via loop 1-3-8-6-1.

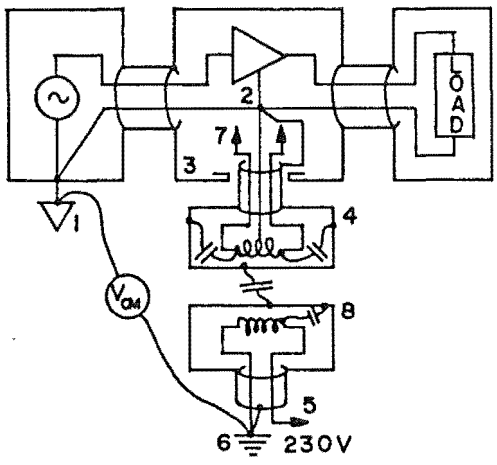


Figure 3.17: Ground-shield connections for a double-shielded transformer.

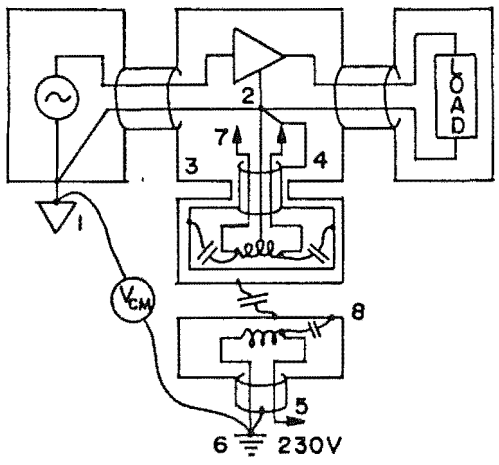


Figure 3.18: Ground-shield connections for a triple-shielded transformer.

(adapted from Morrison 1967)

d) Physical Principles of Shielding Materials

An informative and detailed discussion of the physical principles of shielding materials is given by Ott (1976), and so only a summary of the principles is required within this work to provide quidelines for the application of shields. The shielding effectiveness of a material against electric or magnetic fields, respectively S_e or S_h in units of decibels, is defined in terms of the field strength incident on the shield, E_i or H_i, and the field strength of the transmitted wave emerging from the shield, E_t or H_t, as

$$S_e = 20\text{Log}_{10}\left[\frac{E_i}{E_t}\right] \quad , \quad S_h = 20\text{Log}_{10}\left[\frac{H_i}{H_t}\right] \quad . \qquad (3.16)$$

Two effects contribute to the effectiveness of a shielding material against an incident electromagnetic wave: the wave is partially reflected from each surface it encounters, and it is attenuated (absorbed) as it passes through the medium. The net shielding effectiveness can therefore be considered in terms of the reflection loss, R, the absorption loss, A, and a correction factor, C, accounting for multiple reflections in thin shields, as

$$S = R + A + C \quad (\text{dB}). \qquad (3.17)$$

Table 3.1 indicates the absorption and reflection loses caused by planar 0.8mm thickness sheets of magnetic and non-magnetic shielding materials, for electric and magnetic fields in the common electronic frequency ranges. For each material, its conductivity relative to copper is called σ_r, and its permeability relative to free space is called μ_r. It is seen that:

1) magnetic fields are harder to shield against than electric fields,

2) a good conductor should be used to shield against electric fields, plane waves, and high-frequency magnetic fields,

and 3) a magnetic material should be used to shield against low-frequency magnetic fields.

Table 3.1: Effectiveness of shielding materials (from Ott 1976).

Material	Frequency (kHz)	Absorption loss[a] all fields	Reflection loss		
			Magnetic fields[b]	Electric field	Plane wave
Magnetic (μ_r = 1000, σ_r = 0.1)	<1	Bad-Poor	Bad	Excellent	Excellent
	1-10	Average-Poor	Bad-Poor	Excellent	Excellent
	10-100	Excellent	Poor	Excellent	Good
	>100	Excellent	Poor-Average	Good	Average-Good
Non-magnetic (μ_r = 1, σ_r = 1)	<1	Bad	Poor	Excellent	Excellent
	1-10	Bad	Average	Excellent	Excellent
	10-100	Poor	Average	Excellent	Excellent
	>100	Average-Good	Good	Excellent	Excellent

Key	Attenuation
Bad	0-10 dB
Poor	10-30 dB
Average	30-60 dB
Good	60-90 dB
Excellent	>90 dB

[a]Absorption loss for 1/32-in. thick shield.

[b]Magnetic field reflection loss for a source distance of 1m. (Shielding is less if distance is less than 1m, and more if distance is greater than 1m.)

In practice the leakage through mechanical discontinuities in the shield, like seams, joints, and access holes, is of more concern than the intrinsic shielding effectiveness of the material. This additional leakage can be visualized by considering the circuit theory approach to shielding. Normally the noise field induces currents into the shield which generate a new field that cancels the original field in the shielded area. A discontinuity in the shield

will divert the induced currents from the pattern required for cancellation of the noise field, and therefore reduce the shielding effectiveness. Consideration of figure 3.19 indicates that leakage through a discontinuity is determined by the maximum linear dimension of the discontinuity, and not by its area; the array of holes produce less leakage than a large hole of the same total area. Therefore good electrical continuity should be maintained across all joints in a shield, and shield apertures should be of the minimum practical size.

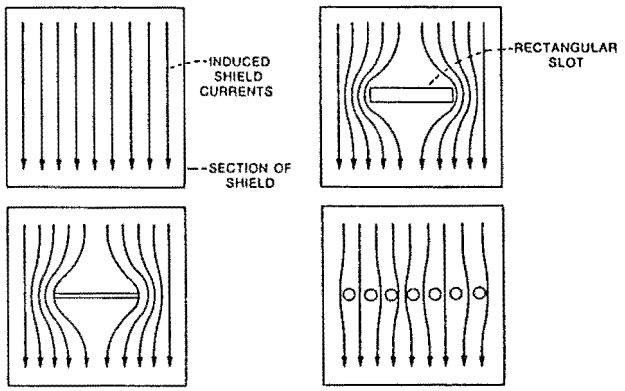


Figure 3.19: The effectiveness of magnetic shielding. (from Ott 1976)

3.2 The MJUO Electromechanical Design

The electromechanical design of the Linear Diode Array detector to be used on the Mount John University Observatory échelle spectrograph must now be produced. Hence the electronic functions to be performed by the system must be determined, their essential grounding and earthing requirements identified, and their grouping into functionally related sub-systems performed so as to ensure their electromagnetic compatability.

3.2.1 Required Electronic Functions

The description of solid-state image detectors in Chapter 1, and in particular that of the Linear Diode Array class in Chapter 2, allows the following list of required system functions to be formed.

1) Power Supplies: The utility power should enter the

system and be conditioned and distributed so as to supply electric power at the appropriate voltage level to the electronic components.

2) Temperature Control and Measurement: The temperature of the array must be controlled so that it is temporally stable at a selectable value. The array temperature and the status of the control process must be available to the detector operator.

3) Control Waveform Generation: The electrical signals which perform the scanning function in the array, and which exercise control over the subsequent electronics, must be generated in sychronization with each other, and with the appropriate control characteristics. It is desirable that those characteristics can be reconfigured when necessary.

4) Scanning Control Signal Conditioning: The signals generated for use as scanning clocks must be conditioned so that they conform to the requirements of the RL936F/30 and RL 1872F/30 diode arrays as given by their specification sheet in appendix 6.

5) Video Amplification, Processing, and Digitization: The information within the video signal must be processed into a form suitable for its subsequent digitization, which requires that the video signal be amplified to a level at which the processing can be performed without contributing to the readout noise. Consideration of amplifier specifications given by any manufacturer will show that single-ended amplifiers generally give more desirable performance than differential amplifiers, for the parameters in common to both types. Therefore single-ended amplifiers and devices will be used wherever possible.

6) Data Acquistion and User Interface: An interface to the system must exist which allows the user flexibility in controlling the detector and its acquisition of image frames, as well as in processing, displaying, and storing those frames.

3.2.2 Earth Connections

As will be described in Chapter 4, the array with its control and video processing electronics are located together

within the 'cryogenic detector head' system module, referred to as the dewar. The dewar mounts onto the échelle spectrograph with its metallic structural components unavoidably making an electrical contact with the spectrograph, and therefore with electrical earth through the telescope. Because the metallic structure of the dewar constitutes the segment of the detector electronics shield that shields the dewar electronics, the grounding and shielding rules in section 3.1.2 require the detector electronics ground to be connected to the detector electronics shield at the dewar. This is because the ground of an electronic system must be connected to the system shield, and that connection must physically occur at the single allowed connection between the shield and an external ground or earth, should it exist. The shield-to-ground connection occurs close to the ground of the array because its video signals are the lowest level and highest impedance signals within the dewar, and therfore are the most susceptible to the EMI being shielded against.

Because single-ended signal processing devices have been chosen, the procedures of section 3.1.2 require that no additional conductive connections be made from the signal ground to either external earth or ground points. This also applies to the shield to prevent it developing a potential along its length due to it becoming one leg of a ground loop. However two additional earth connections within the overall system are stipulated by electrical wiring regulations, whose presence must not compromise the principle of single signal-ground-to-shield and shield-to-earth connections. One of those connections to earth is through the utility power ground, which is isolated by magnetically coupling that power into the signal processing sub-system as described in Section 3.1.2c. The other possible connection could be formed through the communication link to the Data Acquisition and Control sub-system, because that sub-system is earthed to ensure the safety of an operator using its peripherals. That connection will be electrically isolated by optically coupling the signals between the adjacent sides of the communication link. Insufficient volume exists within the dewar for the isolation processes to be located there, and so the interface function

is performed by a separate sub-system. The coupling of the dewar to the other sub-systems is depicted in figure 3.20, as is the isolation between the three earth points within the system.

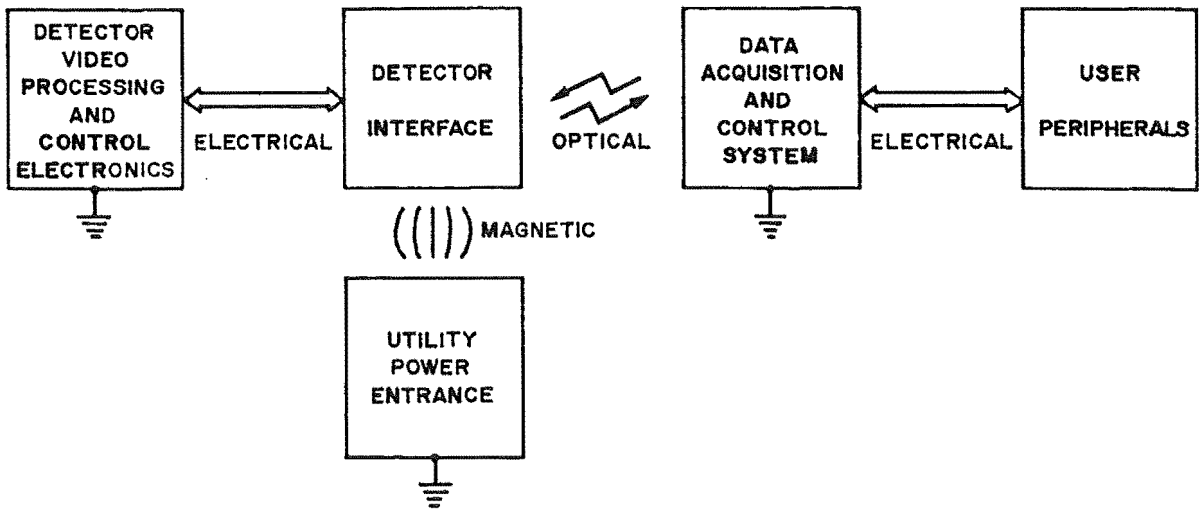


Figure 3.20: Schematic representation of the sub-systems of the MJUO LDA system, showing the coupling between sub-systems and the isolation between the three earth points.

3.2.3 The Electronics Distribution

Consideration of the earth points within the system, and the dewar volume available for electronics, has required an electromechanical design based on the couplings and sub-systems depicted in figure 3.20. For the Acquisition and Peripherals sub-systems, the design represents the radial distribution of power and signals from the Acquisition system to the peripherals, as described in section 7.1.2. The electrical and mechanical construction of the detector electronics and interface, however, require the design to be refined so as to physically represent those sub-systems at the level of their grounding, shielding, and distribution of electronic tasks. The refinement must start with the tasks for the video processing and control of the array, and not with their interface, because the array constitutes the central point for the various detector electronic tasks, and it is the location of the earth point upon which the grounding and shielding depend.

When implemented, the electronic tasks must be electromagnetically compatible with each other, which requires that the appropriate EMC techniques from section 3.1 be applied. To achieve this, the detector electronics will be treated as six tasks, which result from the considerations of section 3.2.1. They are:

1) power supply and control signal interfacing,
2) array control signal conditioning,
3) video-amplification,
4) video-processing,
5) video signal digitizing,

and 6) array temperature controlling.

It is already understood that the interface in task 1 is physically separate from the remaining tasks, which are located within the dewar and electrically connected to the interface. To distribute the dewar tasks, the general EMI emitters and susceptors within the tasks must be identified, as must their principle coupling mechanisms.

The solid-state logic devices supplying control signals to tasks 2,4, and 5 are expected to generate EMI in susceptor devices by common-impedance coupling in shared ground and power distribution lines, as described by section 3.1.1a. Consultation of the application guides supplied by manufacturers of Analog-to-Digital convertors, the principal device of task 5, indicates that those devices also generate considerable EMI by this mechanism. The most probable susceptors of that EMI are devices sharing the same ground as the logic devices, which are processing low-noise tolerance analogue signals like those occurring in tasks 3 and 4. Similarly, both the content of high freqency components in logic signals due to their rapid logic-state transition times, and their large amplitudes make those signals primary emitters for electric and magnetic field coupling as described in sections 3.1.1b and c. Consideration of the equations found within those sections indicates that the most probable susceptors are high impedance level signals, like on the diode-array video lines, and signal lines running close to and parallel with a logic line.

The previous considerations of this section lead to the electromechanical design depicted in figure 3.21 for the

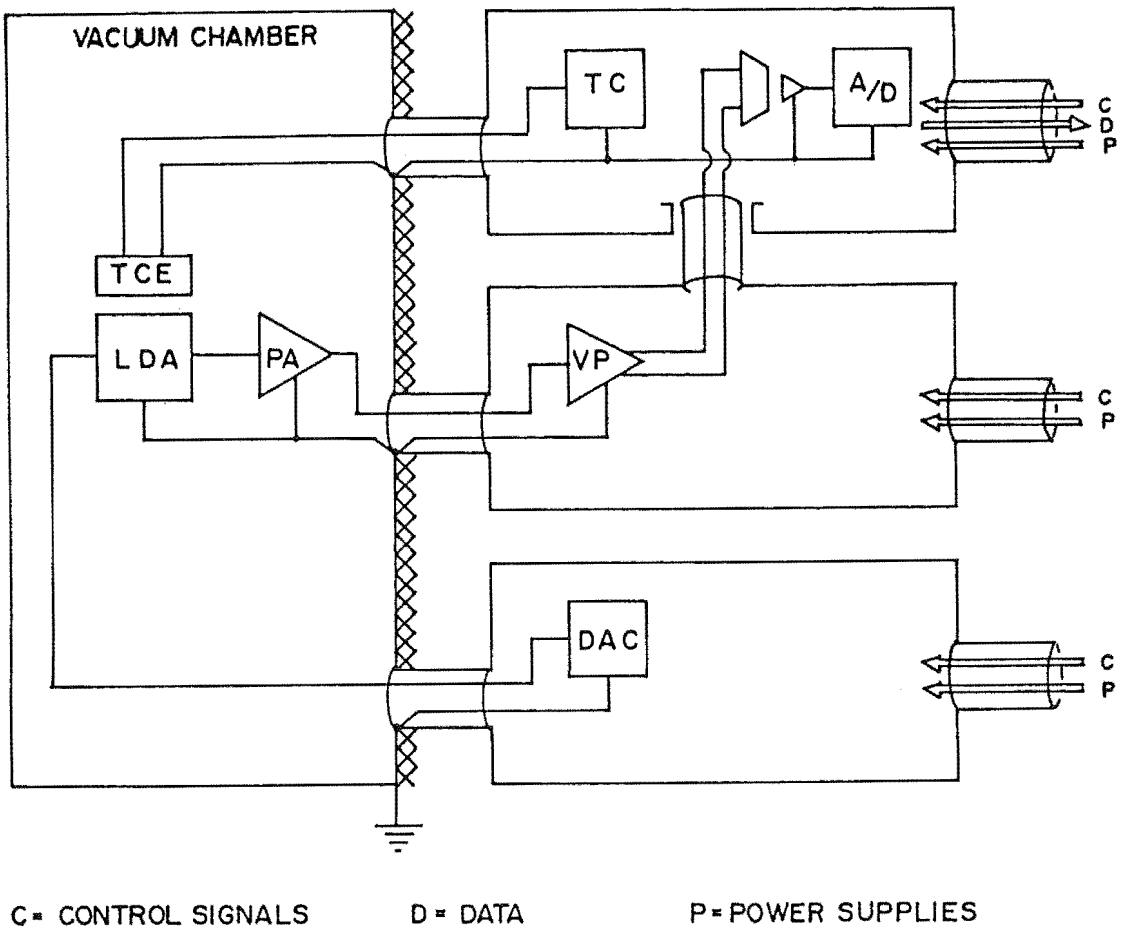


Figure 3.21: Schematic representation of the grounding, shielding, and distribution of tasks within the MJUO LDA dewar, where PA ≡ pre-amplifier, VP ≡ video processing, TC ≡ temperature controller, TCE ≡ temperature controlling element, and DAC ≡ diode array controls.

grounding, shielding, and distribution of tasks within the dewar. The dewar flange plate described in section 4.1.3b constitutes the zero-signal reference plane depicted, to which all other grounds are referenced. The four regions associated with the dewar electronic tasks are for the following reasons.

1) The video amplification is performed within the vacuum chamber in the immediate vicinity of the array so that the video signals can be amplified relative to the zero-signal reference of the array, and so that the length of the high impedance video lines can be minimized to reduce electric field coupling.

2) The amplified video signals are processed in a separate

shielded region due to there being no additional space near the video amplifiers, and are processed into a single differential signal.

3) To prevent the noise of the A/D convertor coupling into the video processing electronics, the A/D convertor is located within a second shielded region on a separate path to ground. However with the video processing and the A/D convertor being on different grounds, section 3.1.2 requires the video processing signal to be received by a differential amplifier at the A/D convertor. The unused space within the shielded region of the A/D convertor is used for the temperature controller because a controller typically operates at very low frequencies which provides it with immunity to the noise of an A/D convertor.

4) The precision conditioning of the diode-array control signals is performed within a third shielded region and relative to a dedicated ground path to the zero-signal plane. This prevents EMI from the A/D convertor, and from the control logic for the video processing, from coupling into the array control signals, and therefore the video signals by the capacitive mechanism described in section 2.1.5.

Figure 3.21 has depicted the grounding, shielding, and distribution of tasks which will allow the incompatible tasks within the system to co-exist with an acceptable amount of EMI. This electromechanical design is compatible with the physical constraints implied in section 4.1.2 for the distribution of electronics within the dewar, and with the requirement of providing shielding against EMI generated externally to the system. The performance of the design must not be compromised by the interfacing of power and control signals into the dewar. Therefore as common-impedance coupling between tasks was controlled by using dedicated ground returns, it should also be controlled by using dedicated power supplies and power supply distribution paths because of the output impedance of each of these. Section 3.1.1c indicates that those power supply paths must be the same as the ground paths to prevent inductive coupling into the power supply and ground lines. Similarly, the distribution of control signals within each task must follow the ground path of the task, and a separate control signal interface to each task will minimize

coupling between the tasks.

Therefore a separate power and control signal interface will be used for each of the three shielded regions external to the dewar. The only electrical contact made between the interfaces is through the dewar so that ground and shielding loops do not exist for EMI to be inductively coupled into. For the same reason, the interfaces are said to be 'floating' because they are not connected directly to earth. The design of the interfaces and their electrical coupling to the dewar will be determined after the general principles for the implementation of the electronic hardware have been set out.

3.2.4 General Electronic Hardware Implementation

The electronic hardware for this system, whose specific design and hardware characterisitcs will be developed in later sections, has been physically implemented with the same general principles. Those principles will now be given so that they will form a foundation for the functional aspects of each area of the electronics as they arise.

a) Printed Circuit Boards

All electronic circuitry is fabricated on double-sided fiberglass printed circuit boards of 1.5 mm thickness. The conductive tracks and areas are of 2oz. copper which has been tin plated, and then solder masked. The component or top side of each board is a solid ground plane, and all the tracks are on the bottom side of the board.

The ground plane is the sole zero signal reference on a board, to which the terminals of components referenced to ground are directly connected. The dc resistance between any two points in the ground planes of the largest boards is less than 0.5 mΩ. At signal processing and logic frequencies, the planar geometry ensures that the inductive reactance and resistive skin effect components of the ground impedance are also kept as low as is practicable. Therefore the level of common impedance coupling in the ground plane will be kept to a minimum. The ground plane also acts as a shield against both inter- and intra-system EMI by shielding the tracks and

components from each other, and by minimizing the loop area of the circuits due to the proximity of the tracks to their ground.

A ground plane can be efficiently implemented because the power supplies are distributed through Rogers Q/PAC QV2 60.2.1 0.5 strip transmision line (bus bar). The power supply distribution is therefore a component rather than a track, and so only signal tracks are required to be routed on the single track side of the board. In the design of that layer, the components which are interconnected by the tracks have the additional role of being used as routes for allowing tracks to cross, and as routes for carrying the signal through the signal processing electronics. Only on rare occasions are zero ohm jumper resistors used to resolve an impasse in the routing of a track.

The bus bar is essentially two strips of metal separated by a thin dielectric to form a transmission line of very low characteristic impedance. Each strip has a row of connection pins separated by 0.2 inches, which are interleaved with those of the other strip. All the pins on one strip are connected to the ground plane, and the power supply is distributed to components through the pins of the other strip. The specifications for the bus bar used show that the impedance of the power supply to ground will be less than approximately 0.5 Ω for frequencies below 100 MHz, which ensures a very low level of common impedance coupling in the power supply lines. Additionally, high frequency ground currents will concentrate in the lowest impedance return path, and so their amplitude will be reduced in the ground plane, which will further reduce common-impedance coupling. It has been found that the bus bar can be bent, with care, to a radius of curvature at least as low as 65 mm over a 300^{o} arc.

The symbols which are used to represent the various component types in the subsequent drawings of printed circuit boards have been given in the symbol table.

b) Active Components

The primary analogue active components are LF356 operational amplifiers. The power supply voltages for the

signal processing electronics are therefore set by their optimum operating voltages of ±15 volts, from which it follows that the allowed range of signal voltages is ±13 volts.

The version of these amplifiers in T099 metal-can packages are used because of the intrinsic shielding of the can, and because their circular symmmetry allows more degrees of freedom in printed circuit board drafting than do the plastic dual-in-line packages. In practice however, one orientation has been found to be optimum for use with the bus bar, and for mounting in dual-in-line sockets. It has pins 4, 5, 6, and 7 on one side, and pins 8, 1, 2, and 3 along the other side. This allows the power supply pins, 4 and 7, to be located next to the bus bar, and the input pins, 2 and 3, to be located away from the bus bar where there will be the most space for related components to be positioned. This is important because to achieve maximum performance from the devices, the physical size of the feedback node must be minimized by placing the feedback components in close proximity to the input pins.

The resistor-capacitor, RC, networks shown in figure 3.22a,b are respectively used to filter the positive and negative power supplies of amplifiers which are conditioning signals that are required to have a low noise content. Their

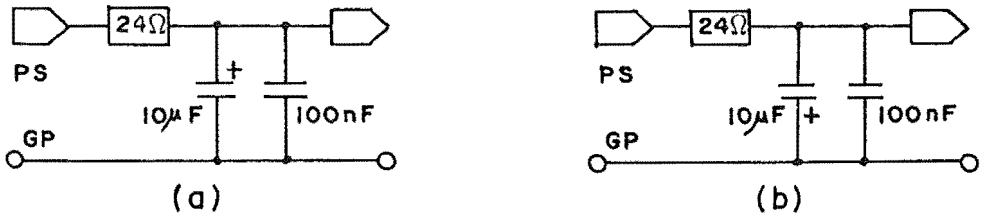
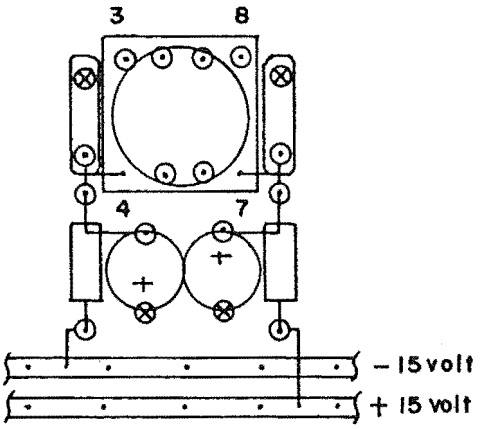


Figure 3.22: The (a) positive, and (b) negative power supply filters for an operational amplifier.

filter frequency of 650 Hz ensures that the power supplies are filtered throughout the upper frequency range of the amplifier where the amplifier power supply rejection ratios, as seen in appendix 7, are low. The filters are physically implemented, as shown in figure 3.23, with the filter capacitors in close proximity to the amplifier power supply pins. The use of the filters, and their proximity to the amplifier, ensures that



Figuer 3.23: The printed circuit board layout of an operational amplifier, and its power supply filters.

the high frequency currents drawn by the amplifier is supplied through the capacitors from the ground plane adjacent to the amplifier, and therefore that common-impedance coupling in the ground plane and power supplies is controlled. The dynamic current supplied to the amplifiers is always less than 1 mA so that the voltage waveform it produces across the filter resistor, which has the characteristic frequency of the filter, can be adequately suppreseed by the amplifier power supply rejection ratio. The two filters for a given amplifier are represented by the symbol given in the symbol table.

c) Passive Components

High quality passive components are uniformly used within the electronics to achieve low noise and high stability. For the following components, either more exact specifications than are supplied by manufacturers were required, or the given consideration will be of significance in applying the component.

Roederstein ERO MK2 metal film resistors, of 0.4 watt maximum power rating, and with 40 ppm temperature coefficients, are primarily used. The temperature coefficients have been measured for a number of these resistors, from a variety of different values, and have all been found to lie in the 0 to +10 ppm range for ambient temperatures of approximately 10^{o}C. However in the critical

positions of precision voltage references, including the bias supply of the diode array, 20k00 Dale PTF60 5 ppm temperature coefficient resistors are used. They have been found to have temperature coefficients which lie in the range of 0 to +3 ppm.

Copal 18 turn top-adjusted variable resistors are used when a variable resistance is required, however Spectral 25 turn devices would have been used if they were initially available. Because variable resistors have high temperature coefficients and are very noisy, they are always padded with fixed resistors so that only the required range of variation centred on the nominal value is available.

ITT tantulum capacitors are used for all filtering tasks within the signal processing electronics because they were found to exhibit the lowest leakage currents, for a given capacitance and voltage rating, in a sample of components from a small sample of different manufacturers. Their equivalent leakage resistance is typically 4 GΩ. For this application, the leakage current must be small because it is drawn through the often high output resistance that is used with the reference to achieve adequate filtration. The high temperature coefficient of the leakage current, exhibited as a voltage variation across that resistance, must not add to the temperature coefficient of the reference.

Diodes are used for the tasks of protecting active circuitry. In particular, negative voltages on large capacitances are found at the inputs of amplifiers used for negative voltage references. A diode between those nodes and the negative power supply is used to prevent the amplifier input voltage from dropping below that of negative power supply during power-down, which would eventually damage the amplifier. However the requirements of the diode leakage current are the same as for the filter capacitor, and so a number of different types were tested. Type 1N4007 were the best in the sample with a leakage resistance of ≈4 GΩ, and so have been selected

3.3 The Interface Chassis

The system requirements and operating principles for

the interface chassis have been determined, and so those objectives will now be implemented in hardware. The general approach to this task will be one of presenting the hardware design and then considering how it achieves those objectives. A general view of a single interface chassis is shown in plate 3.1. The utility power enters the chassis through the utility power conditioning box in the back right corner and is delivered to the primary coil of the transformer at front right. Three of the secondary coils of the transformer supply the three pre-regulating power supplies at the back middle of the chassis, and the fourth supplies the interface electronics which are at the middle front. Control signals communicate with the external sub-systems via the three connectors at back left. The middle connector gives entry to six control signals generated by the Data Acquisition System, which are conditioned for transmission to the dewar by the interface electronics, and sent to the dewar with the previously

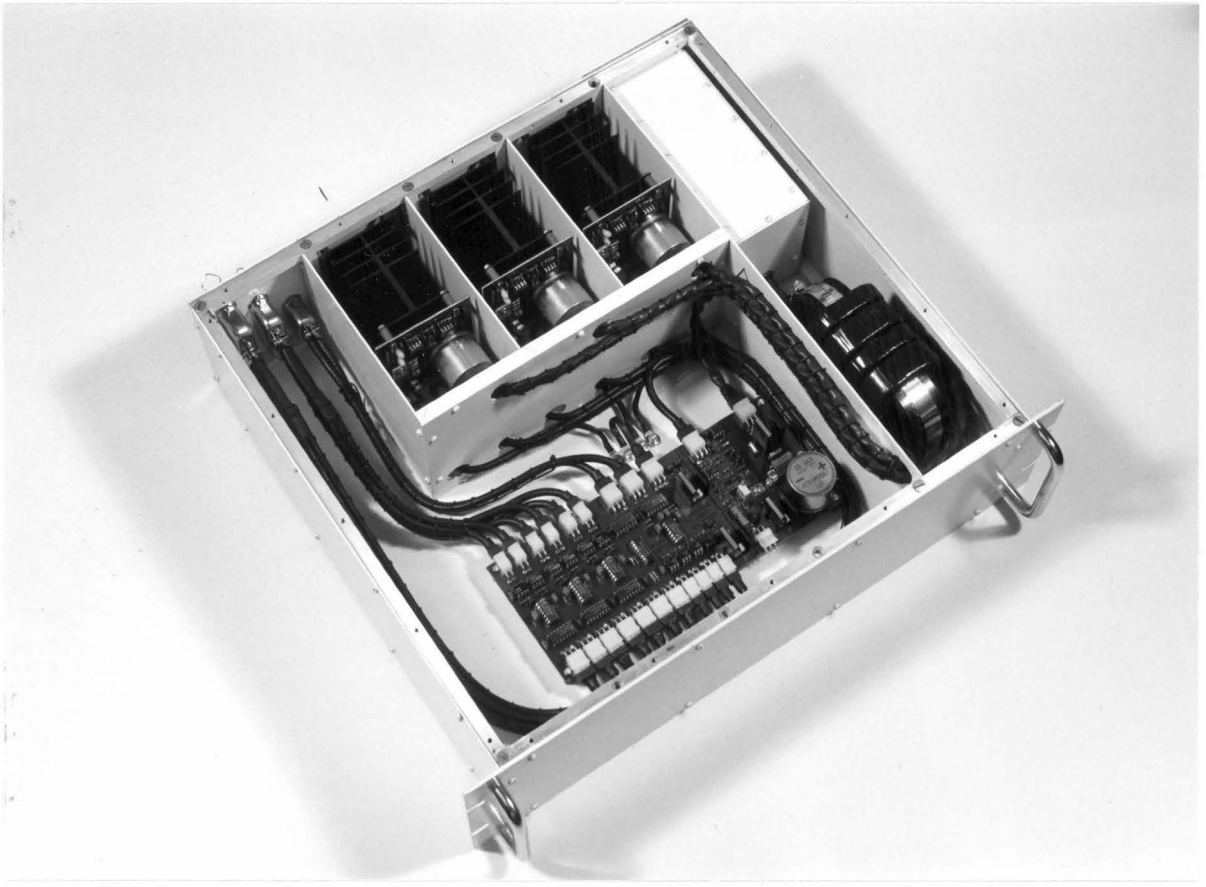


Plate 3.1: A general view of an interface chasis.

mentioned pre-regulated power through the left hand connector. Data from the dewar electronics enters the chassis through that connector and is processed by the interface electronics and sent to the Data Acquisition System with a signal giving the status of the power supplies through the right connector.

3.3.1 The Power Supplies

As indicated in section 3.1.2c, operating power will be supplied to the detector from the utility power lines, and will enter the system by transformer action. Because electric field, magnetic field, and common-impedance coupling decrease with frequency as shown in section 3.1.1, the possibility for EMI emission will be removed from that power by pre-regulating it from an ac to a dc power source before it is transmitted to the dewar electronics. This will also simplify the physical shielding as discussed in section f. The grounding, shielding, and circuitry of that power supply generation and distribution process is depicted for a single positive voltage power supply in figure 3.24. It is the subject of the following sub-sections.

a) Utility Power Conditioning

The utility power enters the chassis through an industry standard connector, is controlled by an illuminated switch, and is fused for safety. A metal oxide varistor between phase and neutral is used to aborb the energy of power line voltage transients which could disrupt the operation of the power supply and subsequent electronics. The power line is then passed through a line interference filter before being connected to the transformer of the power supply. The filter is a passive multi-port network arranged as a dual low-pass filter. One network attenuates the phase or neutral to ground common-mode EMI, and the other attenuates the phase to neutral differential-mode EMI. The operating principle is that of maximizing the common-mode and differential-mode filter-to-line impedance mismatch in the 0.15 - 30 MHz frequency band where attenuation is required.

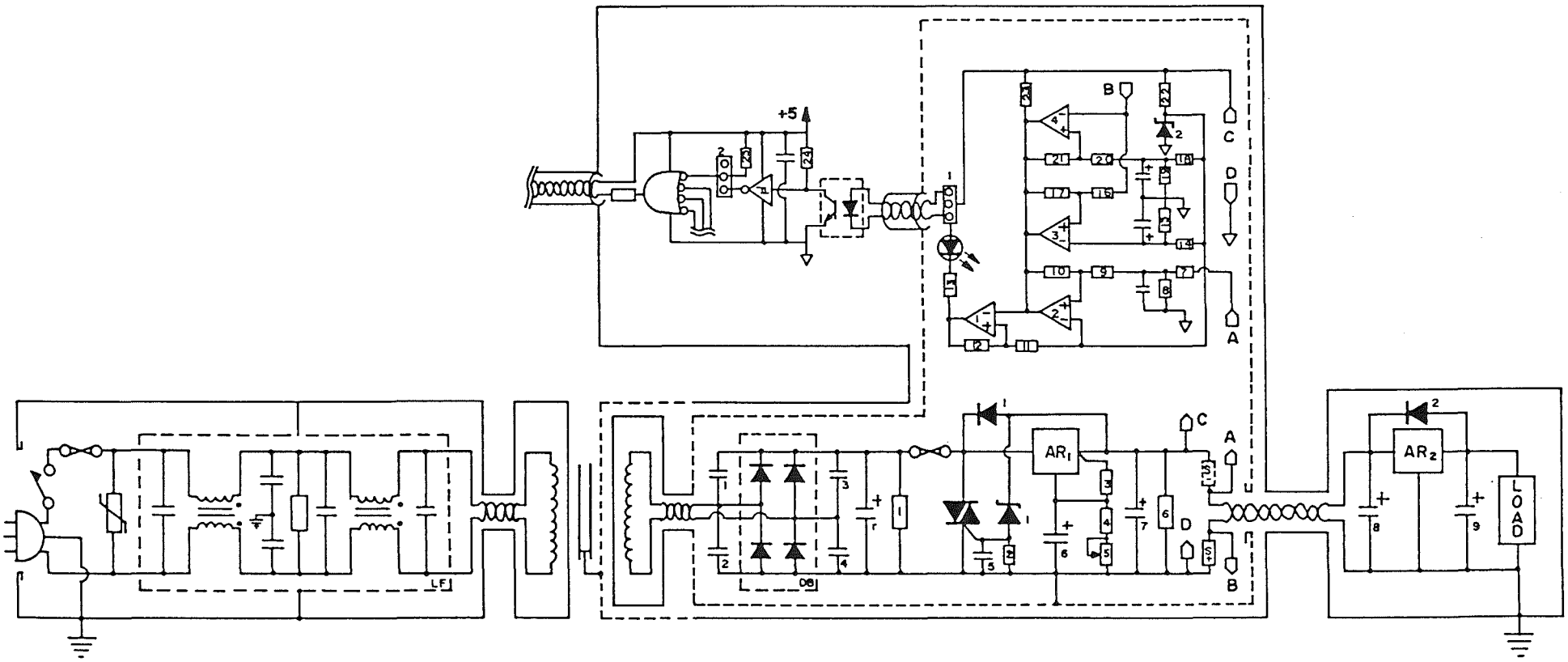


Figure 3.24: Electronic circuit for a single positive voltage power supply.

The requirements for the shield of the power line conditioning components are also those of the primary shield of the transformer, and therefore they are identified as the same shield. That shield is earthed to satisfy electrical safety regulations and the shielding principles of section 3.1.2. Because a significant component of power line EMI propagates as a field around the power line, the line filter is conductively sealed into a bulkhead which allows only signals that have passed through the filter to proceed to the transformer.

b) The Transformers

In sections 3.1 and 3.2, the need for multiply electrostatically shielded transformers was established. The transformers that were designed and constructed are shown in plates 3.1 and 3.2. Those plates show that one transformer is

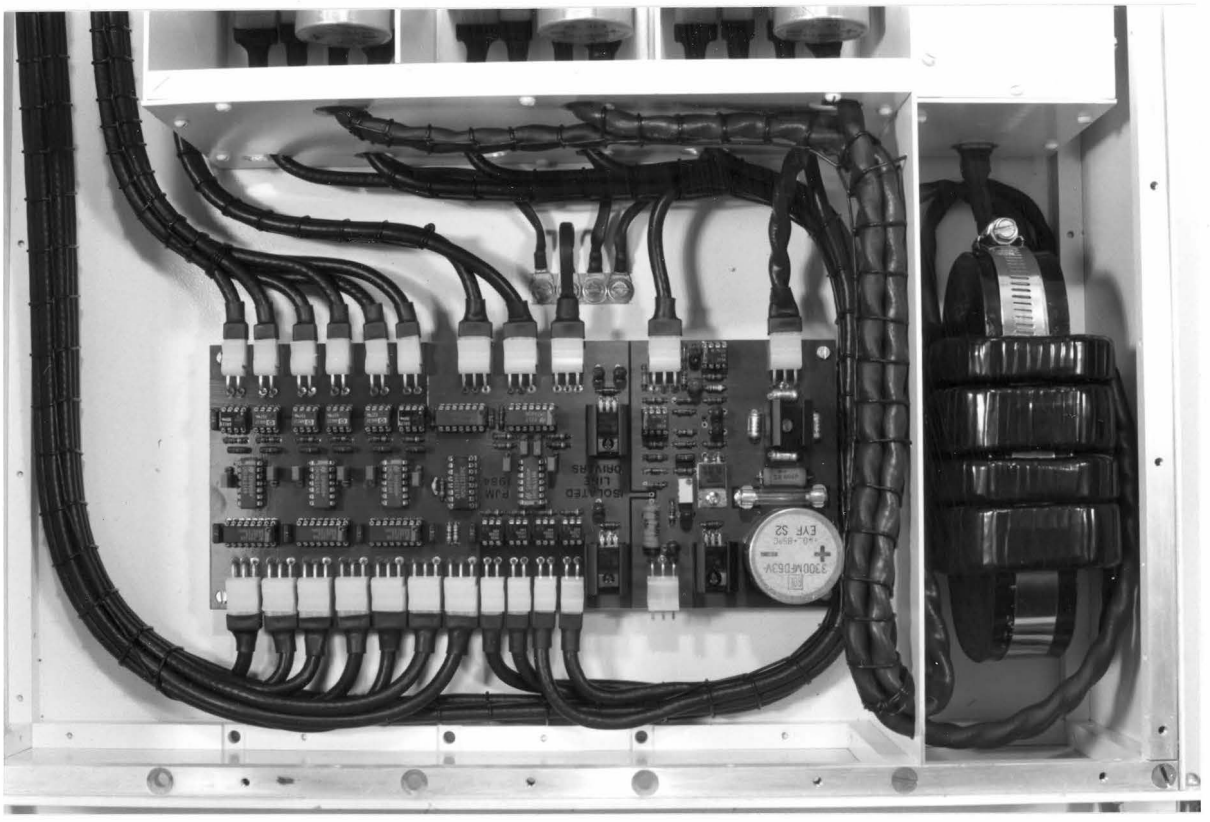


Plate 3.2: An isolated line driver board and triple-shielded transformer.

used per interface chassis, and that the transformer operates four power supplies from its secondary coils. As a result of section c (see below), two coils providing r.m.s. output voltages of V_{rms_sec}, at a maximum r.m.s. output current of I_{rms_max}, are used for each of the following combinations.

$$V_{rms\_sec} = 12.4 \text{ volts at } I_{rms\_max} = 3.7 \text{ amperes}$$
$$\text{and } V_{rms\_sec} = 19.5 \text{ volts at } I_{rms\_max} = 3.2 \text{ amperes.}$$

It follows that the maximum required VA rating of the transformer, the rating with all four secondary coils suppling full load, is 215 VA. The primary coil voltage will be $V_{rms\_prim} = 235$ volts to correspond to the nominal utility power line voltages at the Mount John University Observatory and the Physics Department of the University of Canterbury.

The transformer is constructed on a H.W.R. 70/18/13 C-core with 0.3 mm laminations that satisfies D.E.F. 5193 and B.S. 5347. The cold rolled grain oriented silicon steel core allows 30-40% higher operating fluxes, with a lower iron loss, a lower magnetising current, and less wire per coil than does a traditional E-I core. The properties of this core include

$$3.2 < TPV < 3.54 \text{ turns/volt for } 1.65 > B > 1.5 \text{ tesla,}$$
$$16 < P_{mag} < 30 \text{ volt-amps for } 1.50 < B < 1.65 \text{ tesla,}$$
$$2.5 < P_{core} < 3.6 \text{ watts for } 1.50 < B < 1.65 \text{ tesla,}$$
$$\text{and } TF = 2.8 \ ^{o}C\ W^{-1}.$$

where TPV is the number of turns per volt, P_{mag} is the core magnetization power, P_{core} is the core loss, TF is the temperature factor, and B is the magnetic flux density of the core. In addition to the advantages of these cores listed above, their geometry will be seen to enable electrostatic shielding to be simply implemented, and will minimize the leakage inductance of each coil because the coils can be tightly wound onto the core, rather than on top of each other.

To determine the general coil parameters, the transforming efficiency, e, of the core must be known. It can be deduced from experimental data using

$$V_s = e \frac{N_s}{N_p} V_p \qquad (3.18)$$

where V_p and V_s are the primary and secondary coil voltages of coils with N_p and N_s turns respectively. With a core magnetic flux density of B = 1.58 tesla, the transforming efficiency was measured to be e = 0.972.

Given the three possible coil voltages, and the requirement that each coil has an integral number of turns, the number of turns per volt was treated as a variable in determining the number of turns on each of the coil types. To optimize the performance of the core, it was also desired to hold the magnetic flux density to the lowest practicable value within its allowed range. Using the previously determined value for the core efficiency, the value TPV = 3.290 was determined in conjunction with the following coil parameters

R.M.S. coil voltage:	235	19.5	12.4
Number of turns :	773	66	42 .

For the above TPV value, the values P_{mag} = 20 V A and P_{core} = 3 watts are determined. The physical designs of the coils are constrained by the window area of the core, and by the requirement that the input and output leads of each coil are at the same position on the coil. This requirement is so that twisted pair leads can be attached to the coil, forming a minimum loop area in the circuit containing the coil and power supply electronics. It implies that an even number of layers of turns must be used in each coil, and so the following combinations are used. Six layers of 7 turns each are used for the 42 turn coils, six layers of 11 turns each are used for the 66 turn coils, and 9 layers of 78 turns with a tenth layer of 71 turns are used for the 773 turn coils.

The physical layout of the coils on the core is depicted in figure 3.25, which shows that the core window is completely utilized. Figure 3.26 shows the construction of the coils with a cross-section through one of the sides of a coil. Boron nitride paper is used between the layers, and encasing the coil, to provide inflammable high voltage insulation. The coils are wrapped in PVC insulation tape to provide further insulation, and to bind them together ensuring

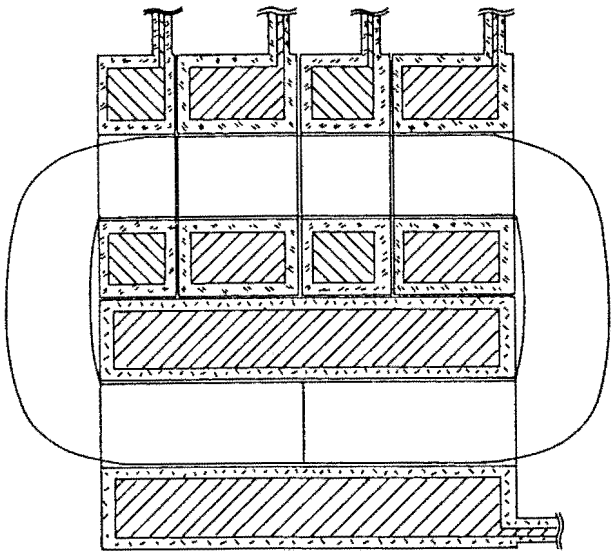


Figure 3.25: Physical layout of the primary coil (bottom), and the four secondary coils (top) on the transformer core.

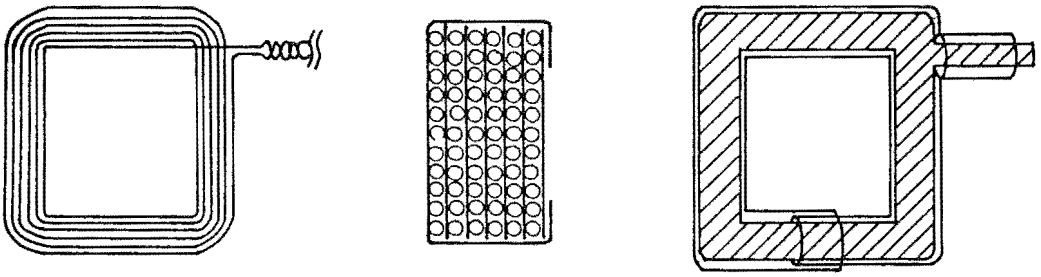


Figure 3.26: Schematic representation of one of the secondary coils (left) showing a side cross-section (centre) and a non-shorted aluminium tape shield (right).

high mechanical rigidity. The coils are wound from enamel coated copper wire of the largest diameters that would fit in the available space. For the primary coils, the diameter is 0.85 mm, and for the secondary coils, the diameter is 1.6 mm. Flexible twisted pair leads are crimped onto the output wires near their exit from the coil. The effective cross-sectional area of each multi-strand lead is the same as as that of the coil wire to which it is attached.

The measured resistance of each type of coil confirms the design values calculated from the length of the mean turn,

the number of turns, and the resistance per unit length of the wire. Therefore the output resistance of the secondary coils can be calculated from

$$R_{os} = R_s + \frac{R_p}{N^2 e^2} \qquad (3.19)$$

where R_p and R_s are respectively the primary and secondary coil resistances. Thus the coil resistances seen by their external circuitry are

Number of turns	:	773	66	42
Output resistance (Ω)	:	4.8	0.14	0.08 .

These values complete those required to determine the maximum power dissipation of the transformer as the sum

$$P_{trans.} = P_{core} + \sum_{coils} P_{coil} \qquad (3.20)$$

where the power dissipation in the coil output resistance, R_{coil}, at maximum r.m.s. load, I_{max_coil}, is

$$P_{coil} = I^2_{max\_coil} R_{coil} . \qquad (3.21)$$

The maximum current loads have been given for the secondary coils, and for the primary coil it is

$$I_{max\_prim} = I_{mag\_prim} + \sum_{sec} \frac{I_{max\_sec} N_{sec}}{N_{prim}} . \qquad (4.22)$$

The subscripts prim and sec refer to the primary and secondary coils, N is the number of turns on the specified coil, and I_{mag_prim}, is the primary coil magnetization current

$$I_{mag\_prim} = \frac{P_{mag}}{V_p} . \qquad (3.23)$$

The maximum transformer power dissipation is therefore 10.0 watts, and so application of the transformer temperature factor indicates that the operating temperature at full load will be 30 C^o above the ambient temperature.

A rigorous interpretation of the shielding discussion in section 3.1 requires that the transformer coils be completely enclosed within the shields. In that case the shielding is referred to as box shielding, and the transformer is said to be of the instrumentation type. Each coil of the

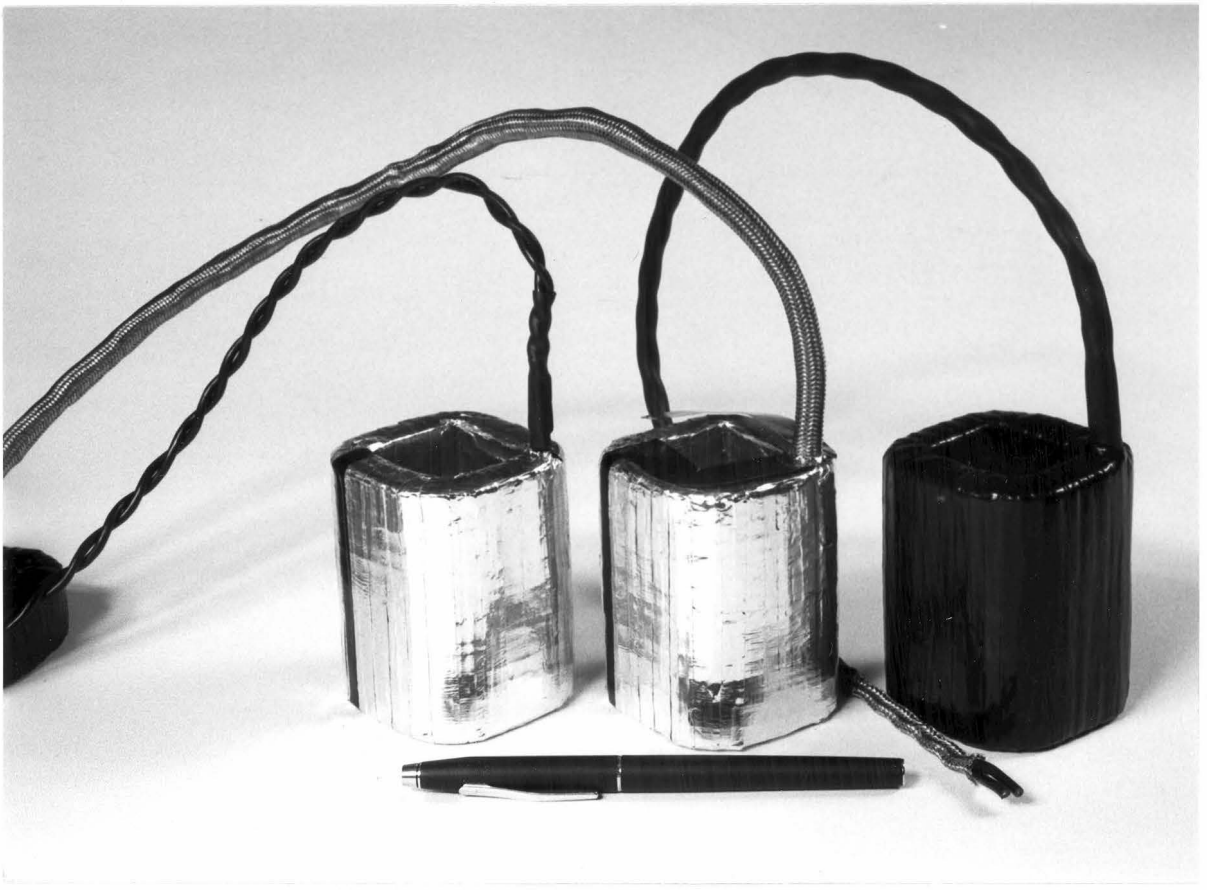


Plate 3.3: Stages in shielding a transformer primary coil.

transformer under discussion has one complete box shield to form a double shielded instrumentation transformer. Three stages in the manufacture of the primary coil shielding are shown from left to right in plate 3.3. The first is the insulated coil with its leads served, the second has the shielding added to the coil and leads, and the third shows the coil completed with insulation over the shielding. The shielding is adhesive aluminium tape which like the PVC tape used for insulation, was wound onto a bobbin for application to the coil. Both tapes are wound with a 50% overlap to effectively give a double layer on the coils. The insulation over the shielding on the leads is heat-shrinkable tubing. As depicted in figure 3.26, the top and bottom layers in the overlap caused by the shielding going around the coil and closing back on itself, are insulated from each other to prevent the shielding from forming a shorted turn around the

Plate 3.4: Stages in shielding a transformer secondary coil.

core. Thus the large current that would flow in such a turn and saturate the core is avoided. Plate 3.4 shows the stages of the shielding process on a 66 turn secondary coil.

A third partial shield is installed in the transformer so that the transformer can be used in the triple shielded configuration shown in figure 3.24. A copper sheet with PVC insulation tape covering its surface is positioned in the window of the core between the primary coil and the secondary coils. That sheet is connected on one side of the window to the core, and together they constitute the second shield of the triple-shield design. Care must be taken not to form a shorted turn around the core with the shielding sheet.

c) Pre-regulation Power Supplies

A transformer secondary coil, whose output voltage will be determined within this section, is shown supplying a pre-regulation power supply in figure 3.25. The power supply uses the diode bridge, DB, to full-wave rectify the ac voltage, and then a capacitor, C_r, to reduce the voltage ripple to an acceptable value. That voltage is then regulated by the solid-state 3-terminal adjustable regulator, AR_1, to give the output voltage determined by the adjustment reference voltage. That voltage is set with the divider chain formed by resistors 3, 4, and 5. By filtering the adjustment voltage, the adjustment capacitor, 6, improves the regulation characteristics, and like the output capacitor, 7, it decreases the output impedance of the regulator at high frequencies. The four capacitors 1-4 are used to suppress noise generated by the bridge diodes as they turn off at the end of each rectifying cycle. That noise would result from the current pulse that occurs due to the change in junction capacitance between forward and reverse bias. The capacitors sink that pulse and thus prevent it flowing in the power supply circuitry where it can produce voltage transients by common-impedance coupling. The remaining components are used to provide protection when a power supply fault occurs, and when the power supply is turned off.

A 'fast-blow' fuse protects the circuitry being powered by the supply from a short circuit of the regulator output to ground, and via the 'crow-bar' circuitry, from the common regulator failure mode of an input to output short circuit. In that case, zener diode 1 detects the output over-voltage condition and turns on the triac, T, to create an extremely low impedance between the fuse and ground. The filter capacitor and secondary coil can then drive a large current through the fuse to blow it and thus isolate the the electronics from the transformer. Resistor 2 ensures that the zener diode provides a low impedance between the supply rail and the triac control gate at the voltages on that gate at or above the triac turn-on voltage. When combined with resistor 2 and the 'off' impedance of the zener diode, capacitor 5

ensures that the triac is not triggered by harmless spikes on the supply rail because once triggered, the power supply must be turned off to reset the triac. The regulator input is protected by diode 1 which conducts the discharge current from the net output load capacitance when the regulator input voltage drops below the output voltage. This occurs during power down, and when the crow-bar circuitry is active. The output discharge resistor, 6, provides the main discharge path for residual charge on that capacitance, but also guarantees a minimum load for the regulator. The input discharge resistor, 1, causes a maximum time constant of $R_1 C_r$ for the discharge of the regulator capacitance during power down. This ensures that the output voltage will decisively drop to zero without relying on the characteristics of the load.

The dewar electronics will operate from power supply voltages of +5 volts, and ±15 volts. Therefore to determine the required transformer secondary coil voltages, V_s, in each case, the voltage drop across each component between the coil and the dewar regulator must be considered. Therefore the general result is

$$V_s = V_o + 2V_r + V_l + V_c + 2V_d \ , \qquad (3.24)$$

where V_o is the dewar regulator output voltage, the V_r are the minimum voltage differentials between the input and output of the regulators, V_l is the line drop in the cables between the pre- and post-regulators, V_c is the peak-to-peak ripple voltage on the filter capacitor when delivering the maximum output current, and the V_d are the forward voltage drops across the legs of the diode bridge when active. The specifications for the regulators and diode bridges in use give V_r = 3 volts, and $V_d \approx 1$ volt. The sum of the line drop and ripple voltage will be specified here to be (V_l+V_r) = 4.5 volts, which allows for a range of possible line resistances, maximum supply currents, and capacitor sizes. Therefore the peak secondary voltages, and corresponding r.m.s. voltages for the specified output voltages are

$$V_o = +5 \ , \quad V_s = 17.5 \text{ volts and } V_{rms} = 12.4 \text{ volts} \ ,$$
$$V_o = +15 \ , \quad V_s = 27.5 \text{ volts and } V_{rms} = 19.4 \text{ volts} \ ,$$
$$V_o = -15 \ , \quad V_s = 27.5 \text{ volts and } V_{rms} = 19.4 \text{ volts} \ .$$

The 25 meter length power supply distribution cables have a

regrettably large line resistance of 2.0 ohms, and therefore a maximum load current of 1.0 amperes is set which gives V_d = 2 volts and a 2 watt maximum power dissipation in the line. This requires that V_r be less than 2.5 volts when suppling the maximum load current. Using these values, the author's programme POWERCAP determines the required capacitance of the regulating capacitor to be C_r = 3300 μF. It has also been used to determine the key parameters for the rectifying and smoothing circuitry that are given in table 3.2 for the +5 volt power supplies, and in table 3.3 for the ±15 volt power supplies. For a specified load current, I_{DC}, in those tables, V_{pp} is the capacitor ripple voltage, I_{rms} is the r.m.s. secondary coil current, and I_{peak} is the peak current supplied to the capacitor in each charging cycle.

Table 3.2: Rectifying and smoothing circuit parameters for a peak capacitor voltage of 14.5 V in the 5 volt power supplies.

I_{DC} (A)	V_{pp} (V)	I_{peak} (A)	I_{rms} (A)
0.25	0.68	4.56	0.86
0.50	1.31	6.24	1.42
0.75	1.90	7.44	1.90
1.00	2.46	8.38	2.33

Table 3.3: Rectifying and smoothing circuit parameters for a peak capacitor voltage of 24.5 V in the ±15 volt supplies.

I_{DC} (A)	V_{pp} (V)	I_{peak} (A)	I_{rms} (A)
0.25	0.70	6.03	0.99
0.50	1.35	8.33	1.65
0.75	1.98	10.00	2.21
1.00	2.58	11.35	2.72

The circuit diagram for the negative power supplies is that of figure 3.24 with the diodes, zener diode, and polarized capacitors reversed within the circuitry. The regulator adjustment circuitry allows for a possible range of 17.0 to 19.5 volts for the 19 volt pre-regulators, and +7.5 to +10.0 volts for the +9 volt pre-regulator. The regulator capacitor can support a maximum r.m.s. current of 5 amperes when operating in an ambient temperature of less than 50 ^{o}C, and has a maximum discharge time constant of 2.2 and 0.7 seconds respectively. The crow-bar circuitry fires at ±20.6 and +10.6 volts respectively.

d) Power Supply Fault Detection

The pre-regulation power supplies monitor themselves for fault conditions with the circuitry given in the top of figure 3.24. That circuitry detects if the output voltage is within an allowed voldage window, and if the load current is within an allowed current window. If one of the 4 possible limits is breached, a logic level is generated to warn the user that a power supply fault is occurring. Because the output signal is optically coupled with the 'light on' state indicating 'no fault', the over-voltage condition is not explicitly measured as the action of the crow-bar circuit will power down the power supply, and therefore indicate a fault because of the resulting 'no light' condition. It follows that if the power supply is off, or if the output signal is disconnected, a fault is indicated. The remaining three limits are checked by comparators which compare the actual level against a reference signal indicating the required limit. Comparator CP2 monitors the low-voltage level by dividing the voltage at A with resistors 7 and 8 so that when A drops below the window limit, the divided level drops below that of zener reference 2 resulting in CP2 changing output state. The load current magnitude is converted into a voltage level by the sensing resistor R_s whose resistance is significantly less than the transmission line resistance. Comparator CP3 monitors the low-current limit by comparing the voltage at node B with the reference level set by the voltage

divider action of resistors 14 and 15 on the voltage from reference zener 2. Comparator CP4 monitors the high-current limit in the same way by using resistors 18 and 19. The comparators are open-collector and switch to a logic low level when a fault is detected. Therefore the three limits are logical 'ORed' into a single fault indicating signal by the connection of the three outputs together. Comparator CP1 is used to invert that signal, light the indicator LED if no fault is occurring, and drive the signal out to an optocoupler. Each comparator has a small amount of hysteresis due to the positive feedback networks like resistors 9 and 10 on comparator CP2. This ensures that noise does not trigger the comparators, and that the transition is rapid when they are triggered.

The fault signals from each of the four power supplies within a given interface chassis are received by optocouplers on the control signal board described in section 3.3.2, have their level transitions shaped by Schmidt trigger buffers, and are logically 'ORed' by the active-low OR-gate into a single fault signal from the chassis. That signal is detected by an optocoupler in the Data Acquisition System as described in section 7.1.3. The signal from any power supply within a chassis will be disregarded by the OR-gate if the mini-jump is set correctly.

The circuit diagram for the negative power supplies is that of figure 3.24 but with connections C and D crossing over, connections A and B crossing over, and the sensing resistor moved into the output lead immediately before node A (as indicated). For all the power supply voltages, the current window is in the 50 mA to 500 mA range. For the +9 volt supplies, the lower voltage limit is +7.5 volts, and for the ±19 volt supplies, the lower limit is ±17.5 volts. The hysteresis for each of the comparators is calculated to lie in the 4 mV to 9 mV range. The low choice of zener reference voltage and the selection of drive current for the optocouplers ensures that the circuit correctly signals a low voltage condition for all voltages below the lower voltage window limit.

e) Dewar Power Supply Regulation

As previously indicated, the pre-regulated power supplies are regulated to the required operating voltages within the dewar electronics, as depicted in figure 3.24. The diode and capacitor are reversed within the circuitry for the negative voltage power supplies. The impedance of the pre-regulation power supplies as measured at the input of the dewar regulators is effectively the parallel combination of the dewar capacitance 8, and the transmission line resistance of R_t = 2 ohms. Their pole frequency is 12 hertz which means that capacitor 8 supplies the current drawn at frequencies above that value, and the pre-regulators supply the current at frequencies up to that value. This effectively implies that all the dynamic currents drawn by the dewar electronics are sourced by the capacitors, and therefore that the activity of the dewar power supplies in that upper frequency range is relative to the dewar ground, and localized within the dewar. Thus the pre-regulation power supplies perform the task of 'trickle charging' the dewar capacitors, and supplying the low frequency currents like that required by the temperature controller described in section 4.2. The interaction of R_t and capacitor 8 also forms a single-pole low-pass filter which attenuates noise on the pre-regulation power supply output, and noise that couples onto the transmission line.

f) The Hardware Implementation

Because each coil of the transformer is enclosed by one box shield, the shield of the primary coil is implemented as the first shield of a triple-shield design, as described in section 3.1, and the shields of the secondary coils are implemented as the third shields of that design. This was depicted in figure 3.24 which shows that those choices are necessary to contain in the coil circuitry the currents driven by the electric fields of the coils. The secondary shield design must enclose the tertiary shields and so in general it is implemented as the metal framework of the interface chassis. However in the transformer, that shield is a partial

shield separating the primary and secondary coils in the window of the transformer, which is connected to the transformer core, and which was described in section b. Given these choices for the shields, the implementation of the power supplies can now be considered.

The utility power conditioning described in section a is physically implemented as shown in plate 3.5. The components are mounted on or within the utility power conditioning box which is an extension of the shield that encloses the primary transformer coil, the first system shield. Therefore the box is insulated from the chassis, the second shield, by a perspex spacer that separates it from the back panel of the chassis onto which it mounts. The line filter is seen mounted in the sub-dividing wall of the box and connected to the twisted pair leads of the primary coil. The shielding on those leads is connected to the end wall of the box as shown in plate 3.2, and therefore to earth as the

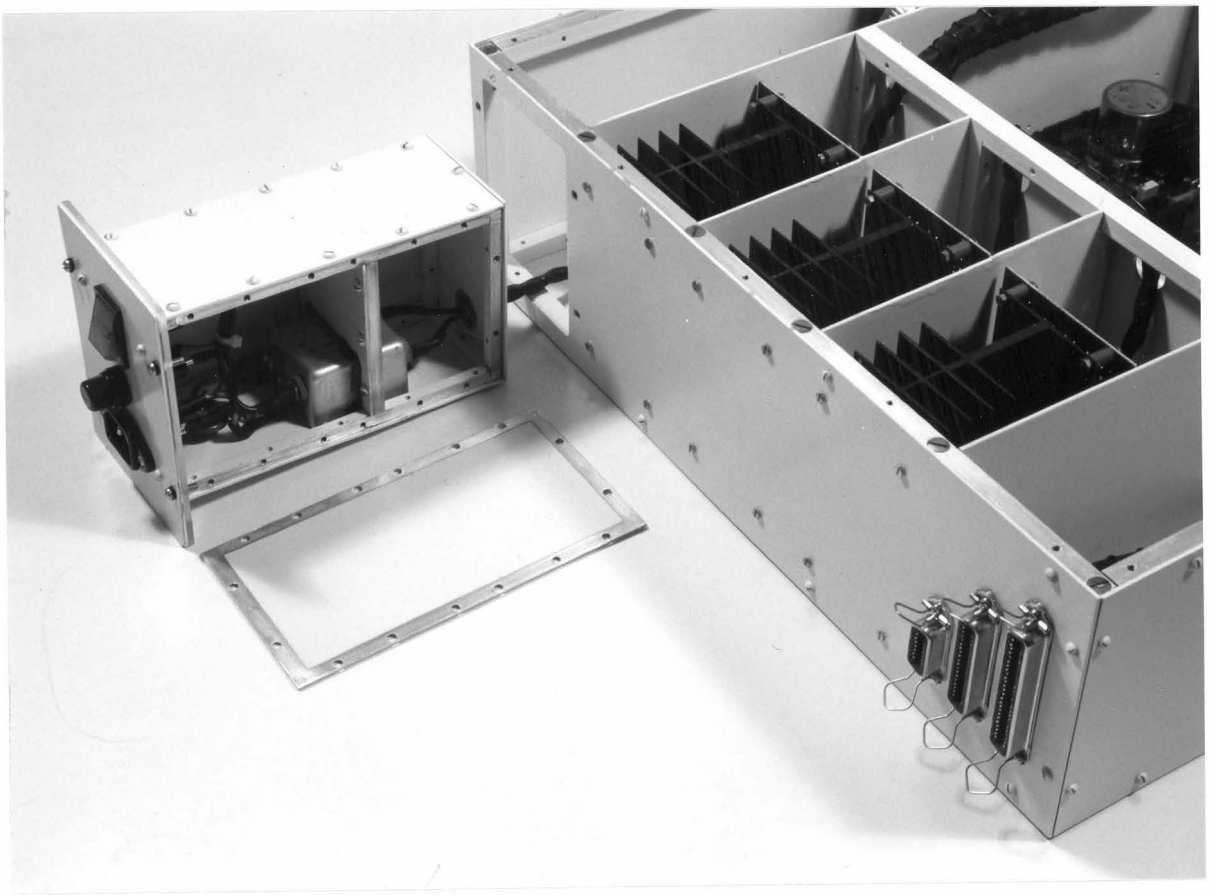


Plate 3.5: Internal view of a utility power conditioning box.

utility power earth from the power cord receptacle is connected to the bottom of the box. Consideration of figure 3.24 and plates 3.5 and 3.2 allows the isolation of the utility power earth, and the confinement of the primary coil electric field to be visualized.

The printed circuit board that is used to implement the pre-regulator circuitry of figure 3.24 is given in figure 3.27 using the same component names. The tracks are on the back

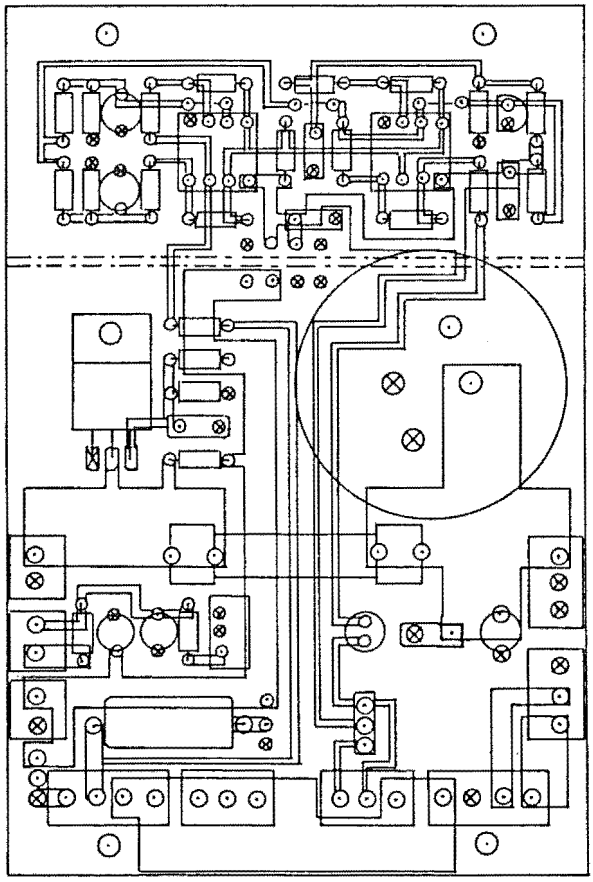


Figure 3.27: Printed circuit board layout for a pre-regulator circuit.

side of the board, and two ground planes are on the front side of the board; one is for the fault detection circuitry at the top, and the other for the power supply circuitry at the bottom. By using the previously given component values, correctly orientating the polarized components, and forming four firm-wired links, this board can deliver either polarity in either of the required voltage amplitudes. The board shown is configured for a positive power supply, and three

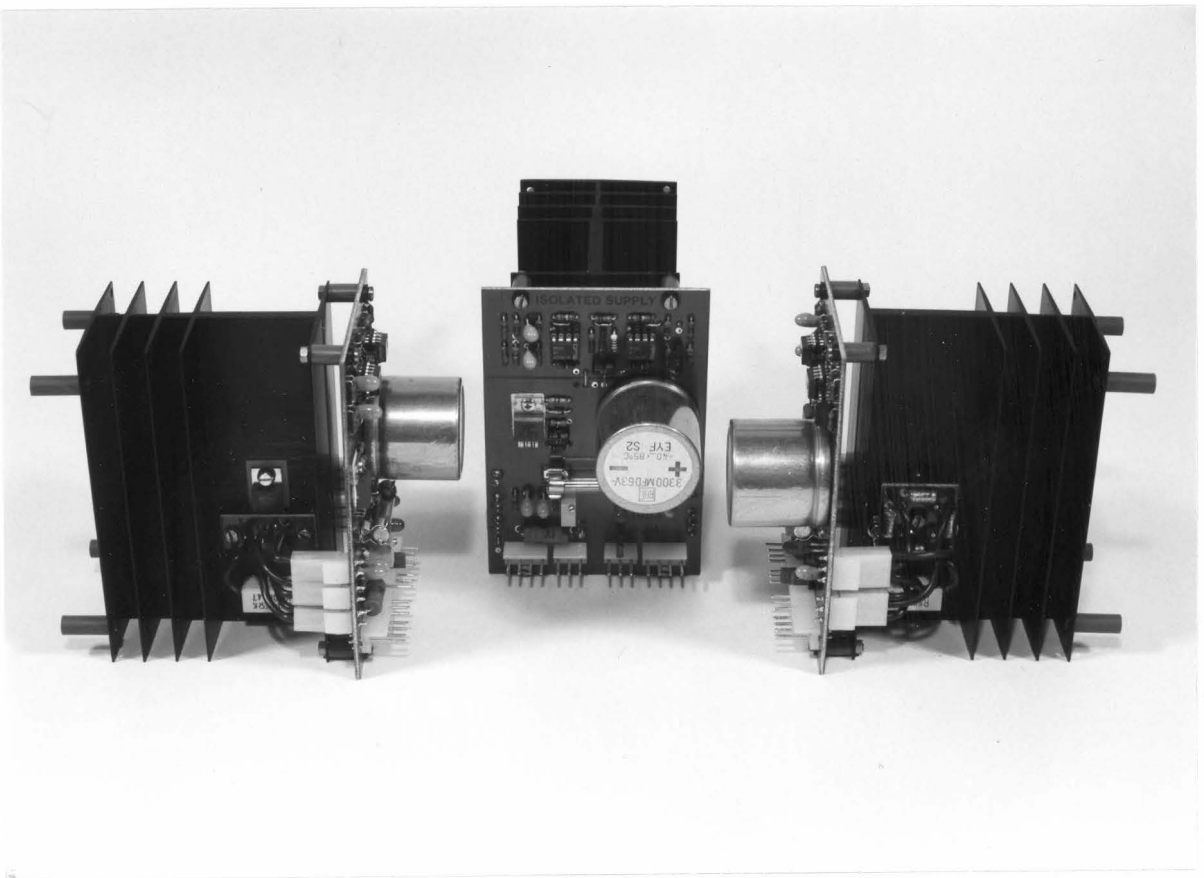


Plate 3.6: Three views of the pre-regulated power supplies.

perspectives of the completed power supplies are shown in plate 3.6. The board is mounted onto a heat sink, as are those components which dissipate power. The left example shows the adjustable regulator with its output bleeder resistor, and the right example shows the diode bridge and suppressor capacitors with the input bleeder resistor. On the printed circuit board the left side connectors from top to bottom are the regulator input, the adjustment circuitry signals, and the output and ground connections. On the right side from bottom to top, they are the diode bridge inputs and the diode bridge ouputs. The bottom four connectors are from right to left the secondary- and tertiary-shield shielded secondary coil inputs, the secondary-shield shielded fault status output lines, the connection to the secondary shield, and the secondary-shield shielded regulator output to the dewar electronics. The right connector allows for a second

shield on the secondary coil to be connected to the chassis secondary shield, and connects the tertiary shield to the power supply ground plane. The metallic heat sink is also connected to the ground plane, and together they complete the tertiary shield which contains the ac high voltage electric field of the secondary coil. Because of the dc output voltage of these power supplies, and the pseudo-dc current supplied by them as previously described, a tertiary shield is not used on the output leads. Plates 3.1 and 3.2 show the routing of the input and output cables to the power supplies, and allow the effect of the compromises in the completeness of the shields to be visualized.

3.3.2 Control Signal Distribution

a) Differential Logic Transmission

The balanced or differential method of distributing logic signals requires a line driver to drive complementary signals down the two wires of a transmission line as depicted in figure 3.28. The line receiver only responds to the

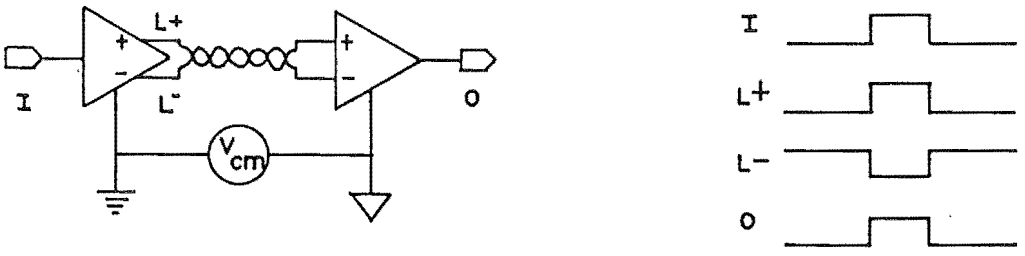


Figure 3.28: Differential distribution of logic signals down a transmission line.

difference in the signal between the two lines, which rejects the common-mode voltage between the driver and receiver as did the analogue differential amplifier in section 3.2. Also of significance is the EMC behaviour depicted in figure 3.29. The mutual inductance and stray capacitance between the external signal line E and each of the transmission lines L+ and L- will cause the signal on line E to equally couple onto those two lines. However the differential signal at the

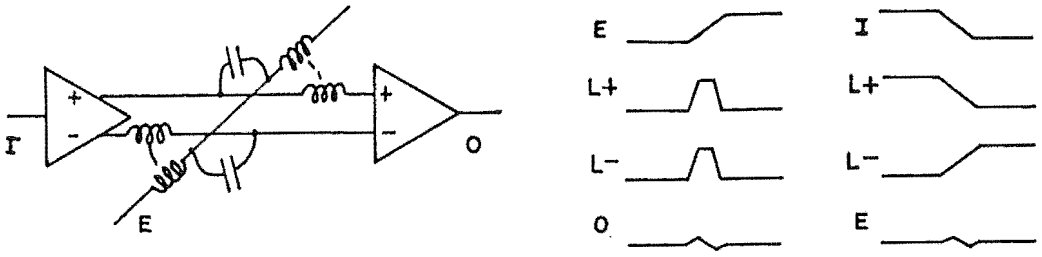


Figure 3.29: Electromagnetic coupling behaviour along a transmission line.

receiver is zero and so the transmission process is not interferred with. Similarly, the balanced signals on L+ and L- result in them coupling no net signal onto line E. Therefore the differential transmission technique rejects common-mode potentials, and is not a susceptor or emitter of radiated EMI. The input currents from the transmission line into the line receiver return to the line driver through the ground, and can therefore common-impedance couple through the ground impedance into other circuitry. If each line receiver input terminal exhibits the same impedance to ground, the return ground current will not have a dynamic component due to the balanced nature of the transmission. Therefore the input impedances should be balanced and as high as is practicable.

b) The Grounding, Shielding, and Circuitry

Each control signal is transmitted from the Data Acquisition System to the dewar with the grounding, shielding, and circuitry depicted in figure 3.30. As described in section 7.1.3, each control signal is generated by a system timing controller, STC, in the Data Acquisition System interface, and is driven out to an optocoupler in the appropriate detector interface chassis. That signal is buffered by a schmidt trigger to ensure precisely repeatable logic level transitions, and a mini-jump allows the option of either inverting or not inverting the signal level. A differential line driver then drives the signal along the transmission line to the dewar electronics where it is received by the line receiver. Resistor 3 and the capacitor terminate the transmission line with its own characteristic

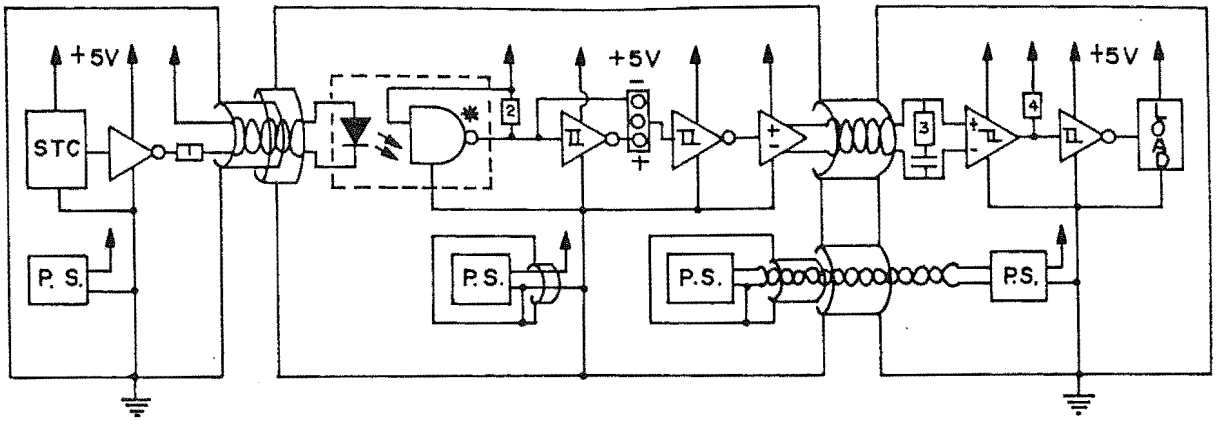


Figure 3.30: Control signal distribution electronic circuit.

impedance to prevent line reflections. The blocking capacitance C passes the dynamic signals, but blocks the high dc current allowed by the low value of resistor 3, and therefore prevents excessive power dissipation in both the driver and transmission line.

The grounding, shielding, and power supply distribution are also depicted in figure 3.30. The shielding of the Data Acquisition System is shown connected to its signal ground and power supply ground at their single connection to earth, but isolated from the interface chassis shielding. Combined with the optical coupling of the signals, this is the isolation between one of the pairs of earth points referred to in section 3.2.2, and the technique used to achieve electromagnetic compatability between those sub-systems being linked. The two power supplies associated with the control signal electronics described in section 3.3.1 are schematically depicted. The pre- and post-regulators of one supply are shown lumped together and supplying the chassis electronics relative to their ground. That supply and the electronics share the same shield, and are joined together at the connection of their grounds to the shield. The pre-regulator and shield of the other supply are electrically floating within the chassis. It supplies its dewar electronics load relative to the dewar ground, and is connected to earth at that point. The primary coil of the transformer and its shield are external to the chassis shield and can again be seen to provide the isolation between the

power ground and the dewar ground that is required.

c) The Hardware Implementation

The control signal interface electronics depicted in figure 3.30 which are within the interface chassis, are located on the main printed circuit board seen in plate 3.1. The layout of that board is given in figure 3.31 and plate 3.2, and shows the interface electronics on the left hand side, and their power supply on the right hand side. The tracks are on the bottom of the board, and separate ground planes for each of the power supply and interface electronics areas can be seen on the top of the board. The transformer secondary coil and its shield enter the top right connector and the shield is connected to the power supply ground plane at that point. The other top power supply connector distributes the fault status signal while the bottom right connector can supply future expansion electronics with the fault checking pre-regulated power. The six control signals arrive on the board from the Data Acquisition System through the six top left connectors. Their shields finish as the cables enter the connector plugs, and capacitive coupling of the signals to the interface board ground plane is minimized by the absence of that plane under both the connector receptacles and the input side of the optocouplers. The signals are interfaced by the three pairs of channels under the connectors, and are line driven out to the dewar through the six bottom left connectors. The seventh from bottom left connector receives the data from the dewar for interfacing with the electronics immediately above it. The data is driven out to a Data Acquisition System optocoupler through the fifth from top right connector. The four fault status signals arrive on the board from the power supplies through the bottom two-pin connectors. Their shielding and isolation from the ground plane of the board is the same as described for the control signal input lines. The signals are interfaced and processed by the electronics above the connectors, and the composite ORed signal is driven out to a Data Acquisition System optocoupler through the fourth from top right connector. The third from top right connector is used to join

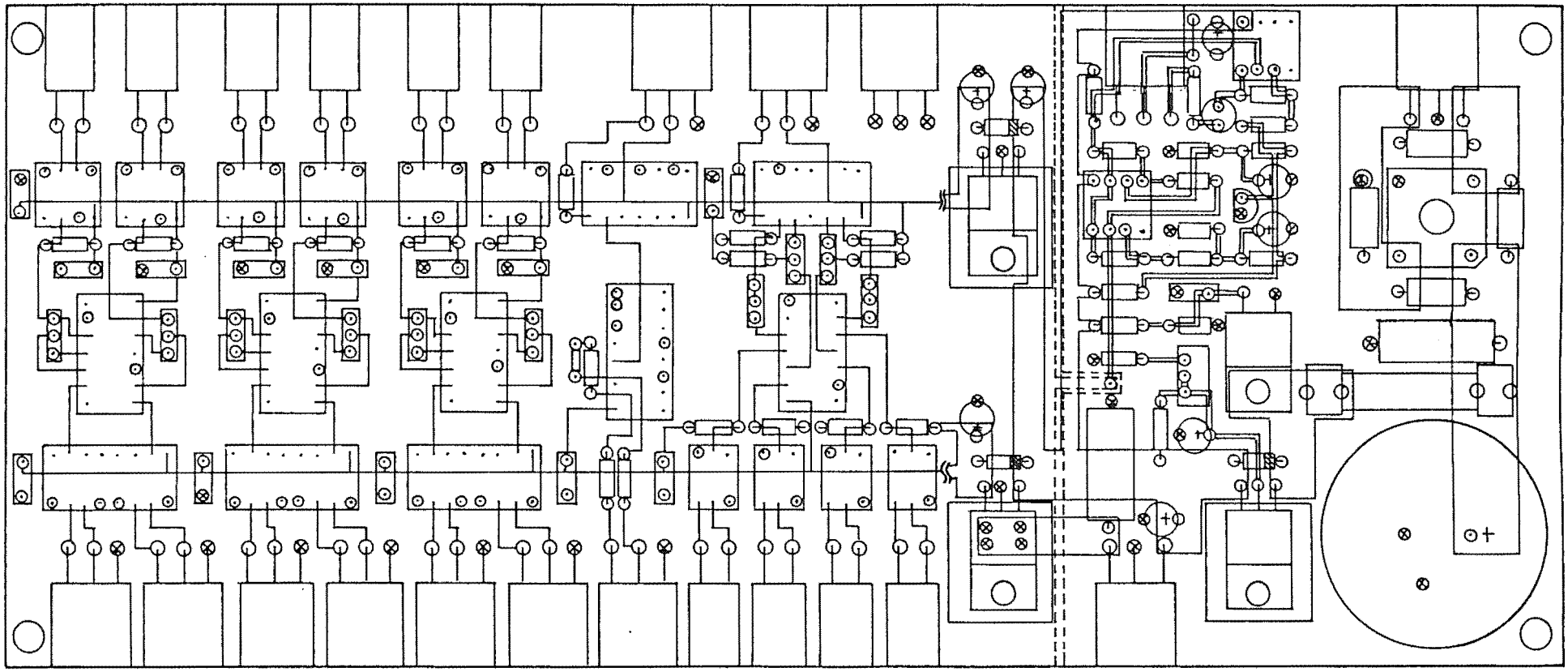


Figure 3.31: Printed circuit board layout for control signal distribution electronics given in figure 3.28.

the ground plane of the printed circuit board to the shield of the electronics, the chassis. That connection is seen to occur at the same place as the three connections of the pre-regulation power supplies to the chassis.

With the exception of the connection to the chassis shielding, all cables connected to the board are of the shielded twisted pair type. Those cables that enter or leave the chassis through the three connectors seen mounted on the back panel of the chassis in plates 3.1 and 3.5, pass through the connector without joining the shields of the cables to the metallic connector cases.

3.4 The LDA Interface and Acquisition Rack

The three interface chassis and the Data Acquisition System are mounted in a standard 19" electronics rack, whose front and back views are shown in plates 3.7 and 3.8 respectively. The Data Acquisition System, to be described in Chapter 7, has its 8" Disk Drive chassis at the bottom of the rack, and its microprocessor chassis immediately above it. The three interface chassis are at the top of the rack, and below them is the Utility Power Switching chassis.

The Utility Power Switching chassis contains two solid-state relays which are individually switched by the Data Acquisition System. The utility power can supply the interface chassis through one of them, and whichever of the spectrograph reference lamps that has been selected through the other.

The front panels of all the chassis are insulated from the rack by a strip of perspex on each of the rack mounting surfaces. The screws which secure the front panels against those surfaces are insulated from the panels to prevent them forming a connection between the panels and the rack. Finally, small gaps between the panels of adjacent chassis ensure that each chassis, when disconnected, is electrically isolated from the other chassis, and from the power earth. This ensures that only intended connections of the electro-mechanical design are made to the chassis.

The cables which interconnect the chassis are visible

Plate 3.7: Front view of the LDA Data Acquistion System and Interface rack.

in plate 3.8. The general cabling principle is that power is on the left hand side, and signals are on the right hand side. Not shown are the two utility power cords which supply the microprocessor chassis and the switching chassis, and the power and signal cables which interconnect the microprocessor chassis and the Data Acquisition System peripherals. Also not shown are the three cables which interconnect the interface chassis and the dewar.

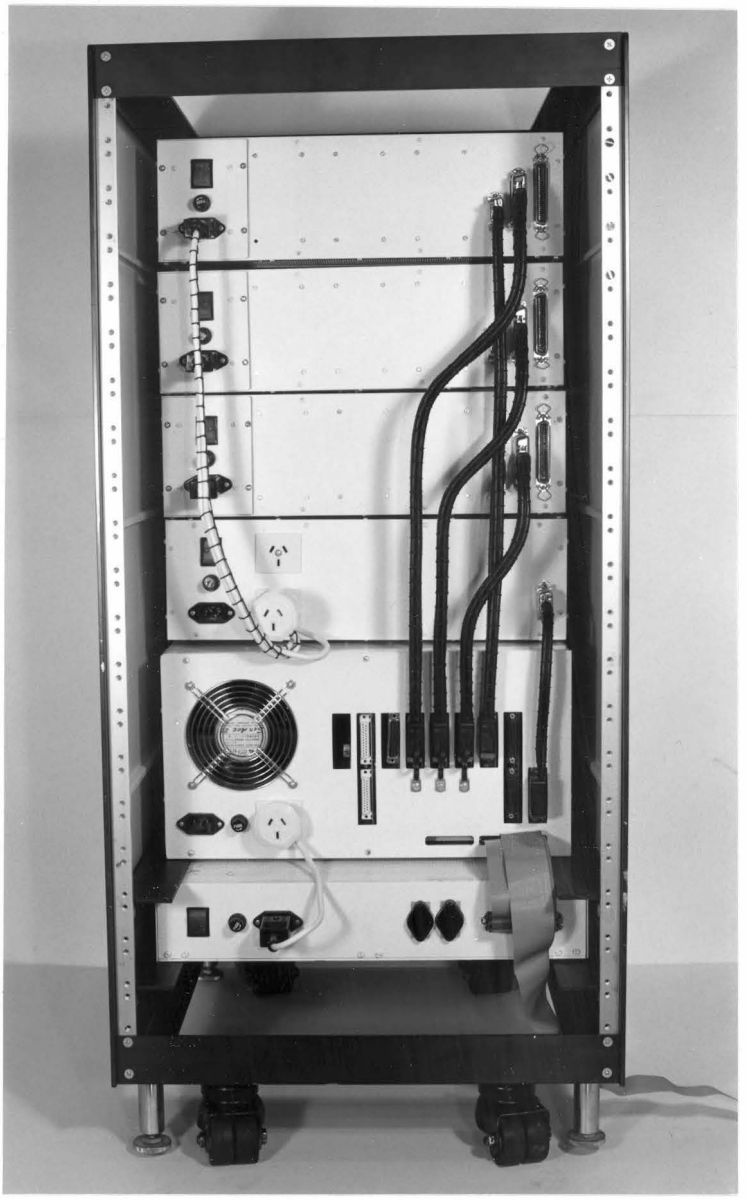


Plate 3.8: Rear view of the LDA Data Acquisition System and Interface rack.

CHAPTER FOUR

THE CRYOGENIC DETECTOR HEAD

The diode array must be both mechanically and optically interfaced to the spectrograph, the readout and control electronics must be appropriately mounted and connected, and the array must be cryogenically cooled to a specified temporally stable temperature. These tasks form the framework of the Cryogenic Detector Head system module, referred to as 'the dewar', which enable its electronic sub-systems to produce the required image frames. The design and specifications of the hardware that constitutes that framework must therefore be given.

4.1 The Mechanical Sub-systems

The operating principle of the dewar is that of a vacuum flask whose inner chamber contains the cryogenic liquid used to cool the array. In the optimum case, the cryogen will only dissipate the heat that originates in the array in order to maintain the required temperature. However in reality, most of the heat dissipated will enter the cryogen through undesirable leakage paths, which requires those paths to be controlled in order to maximize the efficiency with which the cryogen is expended by the cooling process.

The dewar physically divides into three major sub-systems; its tank, lid, and electronics assembly, which will be considered individually. The dewar is shown in plate 4.1, and depicted with a composite cross-section in figure 4.1.

4.1.1 The Dewar Tank

This tank comprises the cryogen storage tank, the thermal coupling between the array and cryogen, and the mounting for the electronics assembly. With the exception of the thermal link, this tank is based upon a Center for Astrophysics (Cambridge, Mass.) design.

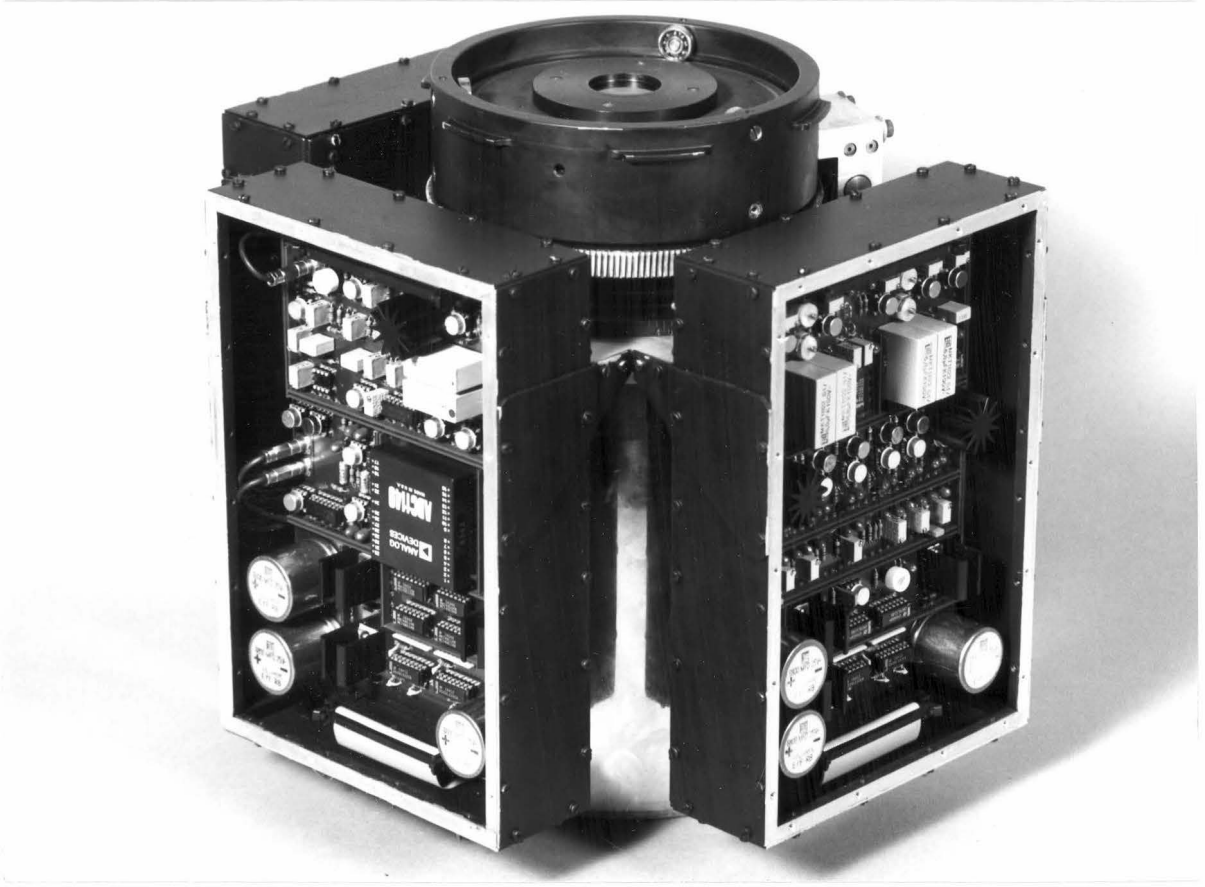


Plate 4.1: The MJUO linear diode array dewar.

a) The Cryogen Storage Tank

The cryogenic liquid is held by a cylindrical tank of 2.0 liter capacity that is mounted within the outer shell of the dewar tank. Both tanks are of welded stainless steel construction. The base of the cryogen tank sits on a PVC mount at the top of a phosphor-bronze support whose five radial fingers spring against a PVC ring on the bottom of the dewar tank. The top of the cryogen tank is held by three PVC cylinders which locate the tank both radially, and vertically due to the bottom spring acting against them. Two stainless steel filling tubes are connected into the cryogen tank via a brass block on the top of the tank. They each pass through a custom nut to seat against a lip within their filling hole through the block. Their outside is vacuum sealed against the lip with indium that is compressed onto the contact by the nut

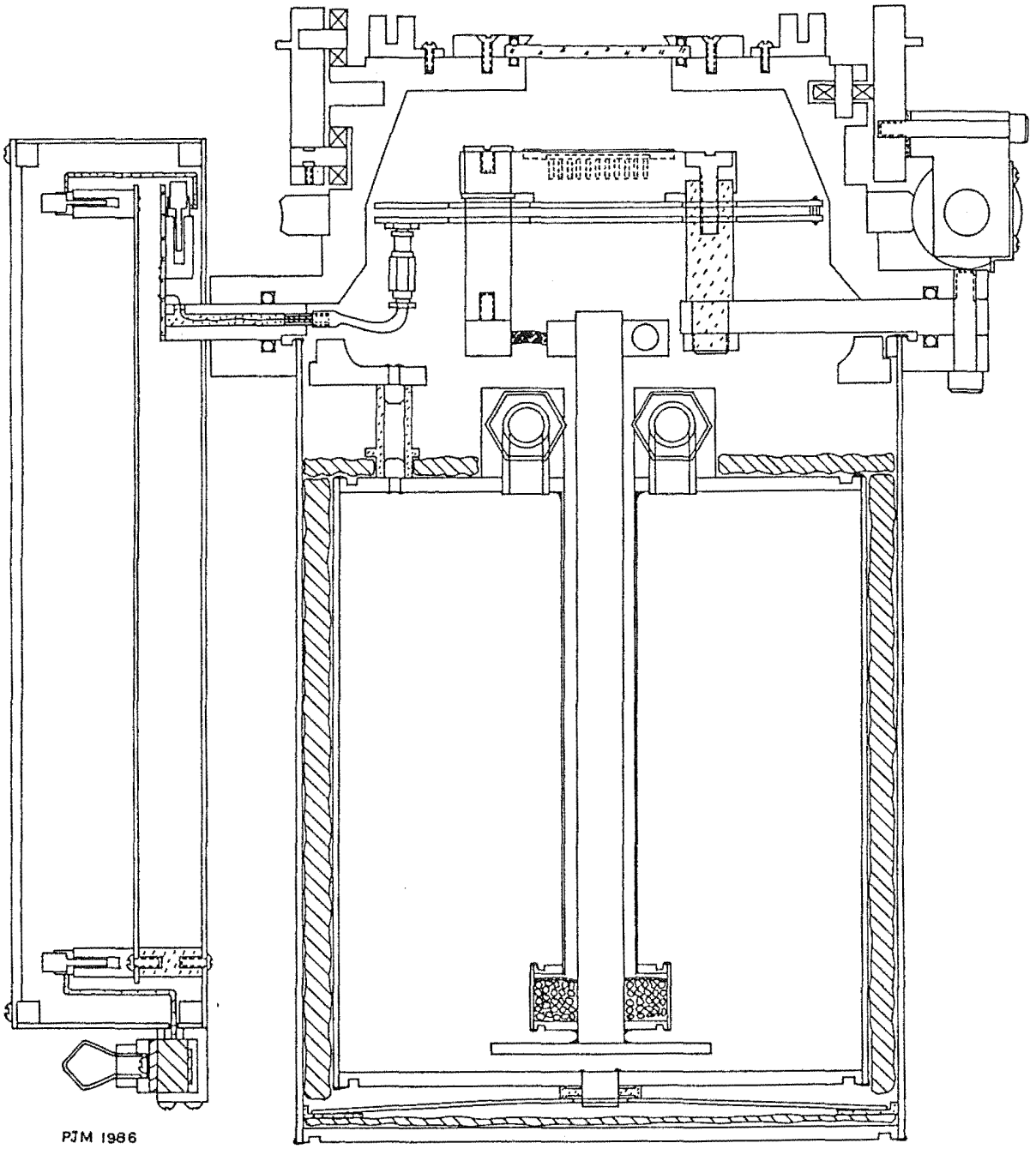


Figure 4.1: Composite cross-section of the MJUO LDA dewar.

as it is tightened. The other end of the tubes pass into the external environment through soldered conections in their individual mountings on the wall of the dewar tank.

b) The Thermal Link

The thermal connection through which heat flows from the block to be dissipated by the cryogen in the cooling

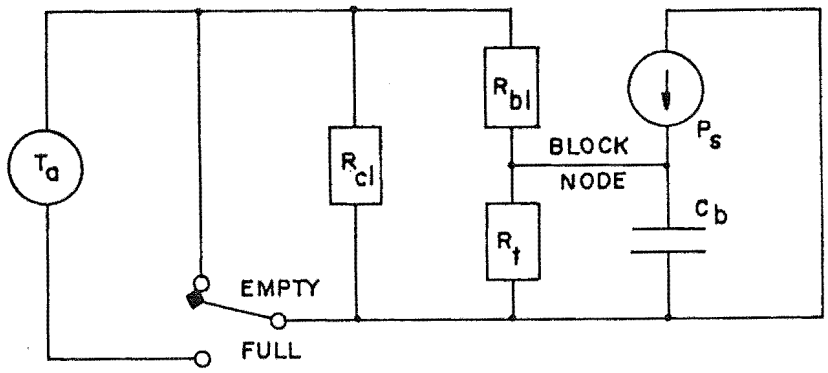


Figure 4.2: Thermal circuit diagram which is used for determining the diode array block temperature.

process is called the thermal link. This process can be represented by the thermal circuit diagram in figure 4.2, and its analysis is the same as for the analogous electrical circuit diagram. The ground potential of the circuit is the cryogen temperature, and the thermal resistance of the link, R_t, connects the thermal capacitance, C_b, of the block to the ground potential. The ambient temperature of the dewar walls relative to the cryogen is the temperature difference T_a which drives heat into the cryogen and block through the leakage thermal resistances of R_{cl} and R_{bl} respectively. These leakage resistances are assumed to be linear, and for the present purpose (see also section 4.2) the power source P_s is the power generated by the array. Therefore the temperature of the block is that of the block node, and is

$$T_b = \frac{T_a R_t}{R_t + R_{bl}} + \frac{P_s R_t R_{bl}}{R_t + R_{bl}} \quad . \qquad (4.1)$$

If the components R_{bl} and P_s do not exist, ie. $R_{bl} = \infty$ and $P_s = 0$, the temperature of the block is that of the cryogen, but in general it is warmer than the cryogen due to heat flowing through the thermal link. The thermal link therefore is a component whose value is determined by the required block temperature.

The absence of cryogen in the dewar is equivalent to the switch being in the position labelled 'empty', with the block temperature being $T_b = T_a$. Filling the dewar with cryogen is equivalent to changing the switch to the 'full' position and results in the block temperature exponentially

decreasing to the value given by equation 4.1, with a time constant of

$$\tau = \left[\frac{R_{bl}R_t}{R_{bl}+R_t}\right]C_b \quad . \tag{4.2}$$

If the ambient temperature changes by ΔT_a while the dewar is 'full', the block temperature will change with the above time dependence by the amount

$$\Delta T_b = \Delta T_a\left[\frac{R_t}{R_{bl}+R_t}\right] \quad . \tag{4.3}$$

The section of the thermal link making contact with the block is the top end of a 60 mm length of 12.7 mm diameter copper rod, known as the heater rod, that fits into a matching hole through the block. A detachable custom copper bolt in the bottom of the rod is connected by a flexible coupling to a copper slit block. At manufacture, the coupling is six lengths of copper braid held side by side by copper rings crimped down around the braid at each end of the coupling to an outside diameter of ≈5 mm. The crimping rings are then soldered into matching holes in each of the bolt and split block, with the rings maintaining good 3-dimensional flexibility in the coupling by preventing solder 'wicking' through the braid. The split block clamps around the top of a 200 mm length of 12.7 mm diameter copper rod known as the cooling rod. Although the cooling rod makes contact with the cryogen along its bottom 3 millimeters of length, the primary contact is through a 60 mm diameter 3 mm thick copper plate sweat-soldered and screwed to the bottom face of the rod. The rest of the cooling rod is isolated from the cryogen within an evacuated 0.25 mm wall thickness stainless steel sleeve which is welded to the rod at the bottom of the cryopump, and open to the vacuum chamber at its top. Assuming that the cryogen tank is more than 20% full and that the dewar is pointing within 70^o of the zenith, this sleeve ensures that the thermal characteristics of the contact between the link and cryogen are neither a function of the quantity of cryogen within the tank, nor a function of the attitude of the dewar. Therefore under the above assumptions, the thermal resistance of the link is a constant and so the only operating conditions on

which the block temperature depends, as given by equation 4.1, are the ambient temperature and the power injected into the block.

For a given thermal leakage resistance to the block, the value for the link thermal resistance is determined by the required block temperature. Adjustment of that resistance is achieved by removing copper from the braid that constitutes the flexible coupling, increasing the thermal resistance and therefore the block temperature. This irreversible process is done iteratively until the block temperature has increased to the required value.

The three detachable metal-to-metal joints within the thermal link each have a film of silicon base heat sinking compound within them to eliminate vacuum gaps and thus maintain a low thermal resistance across the junctions.

c) Thermal Insulation

Thermal insulation is applied within the dewar to control heat leakage into the cryogen so that the time taken to expend a full tank of cryogen, called the 'hold time', can be maximized. Insulation against the conductive, convective, and radiative processes operating in the identifiable leakage paths must therefore be considered.

The components that should be considered for heat leakage paths into the cryogen are the array mounting and the cryogen tank because they are the principal components operating at cryogenic temperatures. Convective heat transport betwen the dewar walls and any of the components at cryogenic temperatures is eliminated by the vacuum within the dewar, to be discussed in section 4.1.1d. The residual leakage into those components is therefore conductive and radiative, and its control for the mounting of the array will be discussed in section 4.1.3a. Conductive heat transport into the cryogen tank through its mounting is minimized by the use of the high thermal resistivity PVC parts described in section 4.1.1a. According to equation 4.4, the rate of radiative transfer to the cryogen tank would be $\approx$0.6W if the tank were gold plated, assuming the emissivity of gold is

≈0.015. A less expensive solution of higher performance was to encase the tank within 12 layers of 'super-insulation'. Each layer is composed of a sheet of aluminium foil over a sheet of fiber-glass matt. The fiber-glass matt provides a very high thermal resistance between adjacent layers of foil due to the large separation between the contacts of adjacent foils on a typical individual fibre, and due to the poor contact between the individual fibres minimizing parallel conduction paths between any typical pair of contacts. Therefore radiation is the only significant heat transport mechanism between the foils, and because they are in series, a typical temperature difference of only ≈18 C^{o} between adjacent foils can be supported for the ≈210 C^{o} temperature drop between the two tanks. This change in temperature difference, from 210 C^{o} to 18 C^{o} between adjacent radiators, is the source of insulation. Both the inside of the dewar tank, and the outside of the cryogen tank are polished to minimize their emissivity to the super-insulation.

d) The Vacuum and Cryopump

The dewar vacuum chamber is the region internal to the lid and tank of the dewar, but external to the cryogen tank. All joints and connections between the non-porous materials delimiting the chamber are either soldered, welded, or sealed with silicon vacuum grease lubricated O-rings. Materials that release gas into the vacuum are said to out-gas, and include paint, glue, plastics, and contaminants like oil and grease on internal surfaces. Therefore all metallic and painted surfaces are cleaned with a de-greasing solvent, and residual gas is baked out of all components by heating with a heat lamp. The dewar is evacuated through a University of Canterbury Physics Department (UCPD) vacuum coupling located under the filling tubes on the dewar tank. The leak detector vacuum pump operated by the cryogenics facility of the UCPD, which can measure vacuum pressures of 10^{-7} torr and greater, will pump the dewar to a presure of $5x10^{-7}$ within 2 hours, $2x10^{-7}$ torr within 5 hours, and ≈10^{-7} torr in ≈50 hours. Experience gained with the dewar vacuum prior to the time of

writing indicates that a vacuum of better than $\approx 10^{-5}$ torr can be held for at least one month after evacuation.

The vacuum pressures given are measured in the absence of a cryogen within the dewar. During cryogenic operation, residual gas whose freezing point is higher than the boiling point of the cryogen will solidify onto the cryogen tank and therefore reduce the vacuum pressure. Also, the cryogen cools the activated charcoal contained by a gauze within a chamber at the bottom of the sleeve surrounding the thermal link. This increases the activation energy for the release of gas molecules chemically bonded to the charcoal, so that once a molecule is absorbed, it is held by the charcoal. Because of this, and the porous nature of the charcoal granules resulting in their effective surface area being many orders of magnitude larger than their external surface area, the charcoal acts as a vacuum pump. It is referred to as a cryogenic molecular sieve material, and the chamber and its contents are called the cryopump. This pump ensures that a high vacuum exists for thermal insulation during cryogenic operation, even though the vacuum pressure may be several orders of magnitude higher when not in operation.

4.1.2 The Dewar Lid

This lid constitutes the optical and mechanical interface to the spectrograph, a section of the shielding for the array and its preamplification electronics, and the top of the dewar vacuum chamber.

a) The Rotation Mechanism

To avoid light loss at either one or both ends of the diode array, the axis of the diode array is required to be parallel to the spectral order. The dewar therefore requires a mechanism for rotating the array about the axis which is perpendicular to the spectrograph focal plane and which passes through the centre of the array. The most significant parameter for this mechanism is the mechanical flexure, and it is required to be smaller than the flexure of the

spectrograph.

The mechanism shown in figure 4.1 rotates the entire dewar relative to the mounting ring that couples the detector head to the spectrograph. The dewar is constrained to rotate coplanar to the focal plane by three pairs of bearings which are separated in their plane by an angle of 120 degrees as subtended from the rotation axis. Rotation about this axis is achieved with a further three radially acting bearings within the plane of the vertical bearing pairs. Each of these radial bearings is at the same distance from the axis as the vertical bearing pairs, but on the opposite side of the rotation axis. One of the radial bearings, and all three of the top bearings in the vertical pairs, are mounted on shafts of eccentric cross-section. The shafts are rotated so that all nine bearings are in firm contact with the particular surface that they run on, and are then locked in position with grub screws. All the bearings are affixed to their shafts with a low-strength 'loctite' bearing retaining compound.

Dewar rotation is performed by a worm-gear affixed to the mounting ring driving a 210 tooth wheel gear on the main body of the dewar lid. The worm gear has an engraved 40 division cyclic vernier which does one revolution in driving from one wheel tooth to the next. The back-lash in the gear meshing is less than 0.5 vernier divisions, or approximately 1 minute of arc.

The mechanical flexure of the spectrograph and detector combination has been determined by comparing a sequence of spectrograph comparison lamp spectra which were taken with the telescope pointing in different directions. The component of flexure parallel to the rotation axis, detected by the change in the full width at half height of the emission lines, is not detectable at the level of 0.25 pixel width changes. The component of flexure parallel to the array axis is detected as a shift in the emission line centroids parallel to the array axis. The worst shift occurs when the direction changes from the array axis being horizontal, to being nearly vertical. In this case it is approximately 2.0 pixels, the same as the 30 μm shift reported by Hearnshaw (1978).

b) Light Trap

No light is allowed to enter the spectrograph through the detector mounting that is measurable by the detector in an integration time of several hours. However light does leak through the rotating head and so the light trap shown in figure 4.1 is used to satisfy the light leakage criteria. The leakage path passes around four 90 degree corners, reflecting each time from matt black surfaces. The light trap decreases the leakage by more than five orders of magnitude.

c) Optical Window

Light enters the vacuum dewar through a 40 mm diameter entrance aperture of 3.5 mm thick optically polished Schott FK5 glass. The transmission loss of this window in the wavelength band delimited by the atmosphere becoming semi-transparent at 310 nm, and by the wavelength being that of the silicon band-gap energy at 1100 nm, is entirely due to the surface reflection losses. The window is supported by an O-ring on each surface, the bottom one of which maintains the vacuum in the dewar. The knife edge aperture that the window cover plate presents to the incomming optical beam is used to shadow the walls of the entrance hole from that beam. This prevents the light of the spectral orders in the converging camera beam from efficiently reflecting and scattering onto the array due to the high reflectance of any surface when illuminated near grazing incidence. Experience gained at this time indicates that a window heater is not neccesary to prevent fogging which would occur when the window temperature drops below the dew point of the air inside the spectrograph.

4.1.3 The Electronics Assembly

The electronics assembly includes the diode array and electronics mountings, the signal connection paths into the vacuum chamber, and the shielding for the dewar electronics located externally to the vacuum chamber.

a) The Diode-array Mounting

The array is required to be operated at a constant temperature of approximately -130 ^{o}C. However the temperature gradient along its signal lines will conduct heat into the array, and heat is also generated within the array due to its internal power dissipation. Therefore the array is required to be mounted on a flexure-free constant low temperature heat sink at the nominal spectrograph focal plane. The implementation of this mounting is an 11.5 mm thick, solid circular copper block of 70 mm diameter and 170 J K^{-1} heat capacity, as shown in figure 4.1, plate 5.1, and in appendix 10. The array sits at the top centre of the block on a leg formed by the two slots through which the signal pins are connected to the external electronics. This leg connects to the main body of the block at each end of the array, and so heat from the array enters the leg from the top, passes along the leg parallel to the array, and exits into the main block. A contact of low thermal resistance is maintained between the leg and the ceramic package of the array by a thin film of a silicon-based heat sinking compound.

The array is held on the leg by the grip of the signal pin sockets into which the array is plugged (see figure 5.5), and by an optical mask attached to the block and in contact with the top of the array. That mask positions a precision rectangular aperture on the array window, of 13.340 mm X 1.135 mm dimensions for the RL936F/30 array. The mask prevents light from striking the array shift registers, and totally masks approximately 20 pixels at each end of the array from light within the f/13.5 spectrograph camera beam.

Any heat that enters the block by conduction or radiation will undesirably expend the cryogen; in the optimum case the cryogen will only dissipate the heat originating in the array in order to stay at the temperature of the block. The mounting of the block is one conduction path: it is composed of three 12.5 mm diameter PVC rods of 25 mm length whose combined thermal resistance is approximately 420 K W^{-1}. The temperature difference across these rods of $\approx$130 K will therefore drive heat at the rate of $\approx$0.3 watts into the block,

an acceptable value. The other conduction paths are the signal lines and the preamplifier printed circuit board, and will be discussed in section 5.3.2c3. Radiation transfers heat from the dewar walls of temperature T_w, to the block of temperature T_b, area A, and emissivity e, at the rate of

$$P_r = Ae\sigma(T_w^4 - T_b^4) \qquad (4.4)$$

where σ is the Stefan-Boltzmann constant. This rate is ≈3.3 watts for a black block, e = 1, and so the block is gold plated to reduce this to an acceptable rate of ≈0.1 watts. The mask is required to be matt black to absorb stray light, and so its surface area must be as small as practicable to minimize its absorption of thermal radiation which would be transferred to the block.

The conduction path out of the array, as described, is such that a thermal gradient can exist along the mounting leg, producing uneven cooling of the array, and the possibility of an undesirable temperature gradient within the array electronics. Investigation of the possible performance degradation has not been carried out; however Tull (1983) has designed the mounting for the McDonald Observatory 'Octicon' detector arrays to minimize this problem. This problem can be avoided if the conduction path of the mounting is directly away from the bottom of the array rather than parallel to it.

b) The Mounting Flange

The mounting flange which is depicted in figure 4.1 and appendix 12 is an 11.5 mm thick milled aluminium plate on which the cold block mounting pillars are located (see also section 4.1.3a), to which the electronics boxes are mounted (see section 4.1.3d), and through which the signal lines (see section 4.1.3c) pass from the vacuum chamber to the external electronics. The purpose of the flange is to enable the electronics to be assembled and tested as a single module in the absence of the dewar lid and cryogenic tank. The flange also provides a smooth finish on its top and bottom surfaces on which the vacuum O-rings in the dewar lid and cryogenic tank can seal.

c) The Co-axial Feedthroughs

The signal exchange between the electronics internal and external to the vacuum chamber is via 24 swg tin coated copper wires which are vacuum sealed with Araldite glue into ≈3 mm diameter holes which pass through the flange. A hollow brass sleeve is screwed into the end of each hole within the chamber, protruding ≈6 mm into the chamber, and secured to the flange by a locking nut. Each wire is insulated with a layer of heat-shrinkable tubing while in the chamber, which finishes after the wire has passed through the sleeve. Each insulated section of wire is then shielded with copper braid to form a co-axial wire, with the braid bound to the sleeve at the flange end, and insulated with a layer of heat-shrinkable tubing. The free end of each co-axial wire is terminated with a Sealectro 'Conhex miniature co-axial plug' for connection to the preamplifier printed circuit board. Therefore each wire is co-axial between the preamplifier board and its exit from the flange because the flange, at zero signal potential, is a continuation of the braided shield.

To achieve the glued vacuum seals, the wire and flange holes were first cleaned with a de-greasing solvent. The glue and flange were preheated to 35 ^{o}C with heat lamps operated by a temperature controller that used a thermocouple to measure the flange temperature. The top exit of the hole was sealed off using a threaded nylon stopper through which the wire passed, and the heated glue was forced into the adjacent hole exit with a syringe until it flowed from the other end between the insulated wire and sleeve. Heating the glue expels air bubbles and enables it to flow, and heating the flange prevents the glue from cooling on contact with the flange. The temperature of the flange was maintained for 24 hours after the above operation to ensure that the chemical process which sets the glue would go to completion, preventing out-gassing into the vacuum chamber.

d) The Electronics Boxes

An electronics box is mounted on each of the three

interface areas of the flange plate, which can hold a rectangular printed ciruit board of 160 mm X 210 mm dimensions, and allows the components on the board to be up to 35 mm high. Each board is supported on its four corners by insulating stand-offs, and is connected from an insulation displacement socket at the bottom of the board, via 50-way ribbon cable, to an Amphenol 57F series connector external to the box. Within each box an insulation displacement socket at the top of the board connects signals via 64-way ribbon cable to the dewar interface board, whose layout is shown in appendix 12, through a similar socket. A minimum of 44 ribbon cable wires connect the ground planes of the two boards, and a gold plated area of the interface board ground plane is firmly screwed to the edge of the interface area on the zero-signal potential flange plate. The total ground resistance between the electronics board and the flange plate is less than 1 mΩ. Signal tracks on the interface boards connect the appropriate socket pins to the co-axial feedthrough wires as they exit the flange. Two ribbon cable wires are used for signal lines and four are used for power lines, giving a total line resistance between the preamplifier and external electronics of 15 mΩ and 10 mΩ respectively. The interface board ground plane is on the side of that board which shields the signal and power lines from any undesirable coupling with the main electronics board.

The electronics boxes form the external shield for the electronics that they contain, as described in section 3.2.3, therefore all contacts between the 1.5 mm thickness aluminium cover plates and the box framework of 6 mm X 6 mm aluminium are conductive metal to metal joints. The shielding on the cables entering the external connector are joined through the connector to wires 1, 2, 49, and 50 of the 50-way ribbon cable, which are connected to the box as a continuation of the shield, and not to the electronics ground plane.

4.1.4 The Cryogenic Performance

Key parameters by which the cryogenic performance of the dewar can be quantified are its thermal leakage rate, its thermal time constants, and those conditions affecting the

natural temperature.

a) Thermal Leakage

The net power dissipation by the cryogen can be determined by measuring the rate at which the combined dewar and cryogen mass decreases due to the vaporization of the cryogen. That rate is the gradient of the mass versus time curve plotted in figure 4.3, whose data were collected with the electronics running, the temperature controller off, and the dewar stabilized at its natural temperature. Therefore the power dissipated by the cryogen is 5.6 watts, the product of the mass loss rate and the 1.992×10^{-5} J kg^{-1} latent heat of vaporization for the liquid nitrogen cryogen.

Two thermal leakage paths can be identified over which more control should have been exercised in order to reduce the high level of leakage. One path is through the filling tubes which provide a metallic conduction path between the dewar tank walls, which are at ambient temperature, and the cryogen tank at the temperature of the cryogen. The other paths are all conduction paths from the flange to the block, and are the preamplifier printed circuit board and its signal lines to the array.

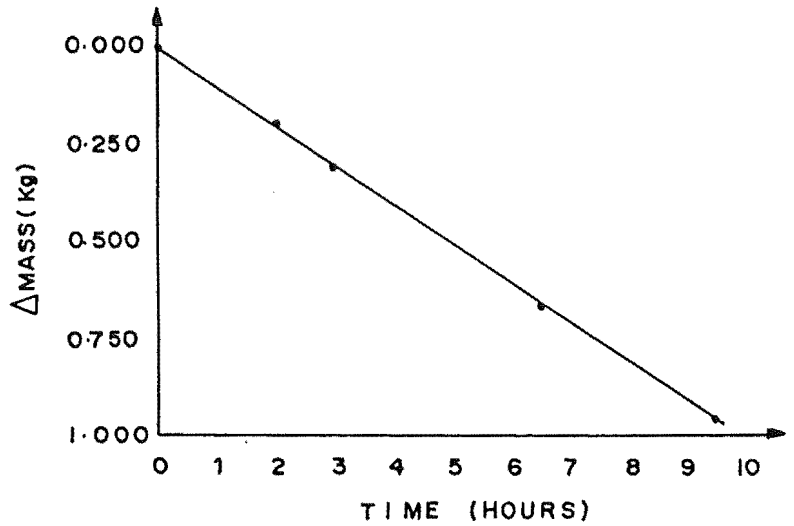


Figure 4.3: Rate of change of cryogen mass which is used for determining the power dissipation by the cryogen.

b) Thermal Time Constants

The thermal leakage rate found in section 4.1.4a will result in a typical hold time of ≈18 hours, which sets the practical requirement of the tank being topped up during operation at one half day intervals instead of a more desirable one day interval.

The temporal response of the block temperature to a step change in the difference between the ambient and cryogen temperatures was modelled in section 4.1.1b. The most common case is that of filling the dewar with cryogen, whose response is called the cooling curve. A typical cooling curve is given in figure 4.4; its initial temperature was 24°C, adjacent data points are connected with line segments for clarity, and the curve can be judged to have the predicted exponential behaviour with a time constant of ≈2250 seconds. This time constant provides stability against high frequency changes in the block temperature, and its large value will be found in section 4.2 to be of significance to the performance of the block temperature controller.

Using the thermal capacity of the block that was given in section 4.1.3, the net thermal resistance between the block and cryogen is found from equation 4.2 to be ≈12.5 $C^{o}\ W^{-1}$.

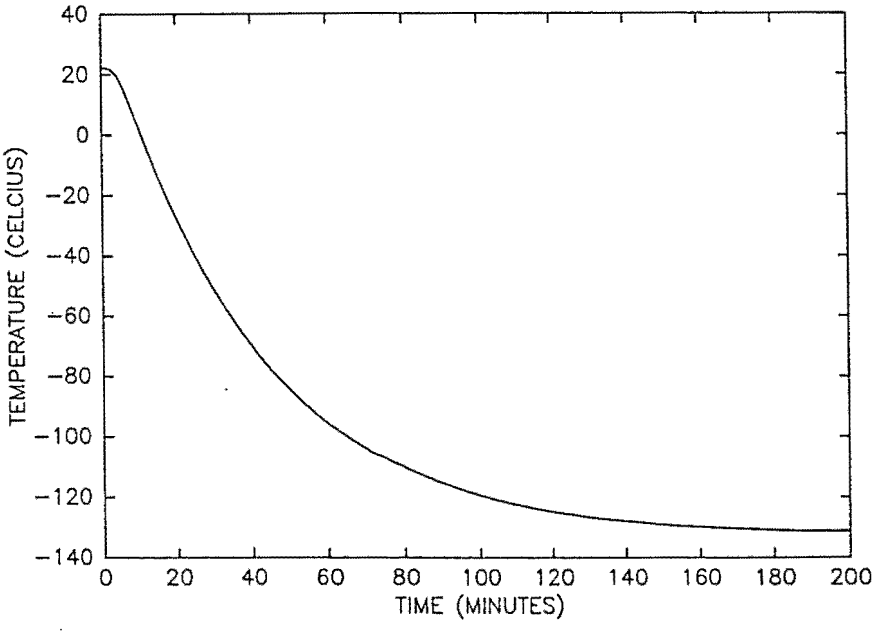


Figure 4.4: Typical cooling curve for the MJUO dewar.

c) The Natural Temperature Dependence

The design given in section 4.1.1b for the thermal link was intended to make the natural temperature of the block independent of both the quantity of cryogen within the tank, and of the attitude of the dewar. Measurements of the natural temperature over the range of operating conditions specified in that section have confirmed the independence at a tolerence level of $\approx 0.3\ C^{o}$. Therefore equation 4.1 indicates that the block temperature is only dependent on the heat injected into the block, to be discussed in section 4.2, and on ambient temperature changes. To determine the constant of proportionality in equation 4.3, which relates the change in ambient temperature to the change in natural temperature, the ambient and block temperatures were simultaneously recorded every ten minutes during a 21 hour interval. The constant was calculated as the quotient of the amplitudes of variation from the respective sources, due to the 11 C^{o} diurnal ambient temperature variation, which allows equation 4.3 to be expressed as

$$\Delta T_b \approx (0.45)\Delta T_a \ . \qquad (4.5)$$

4.2 The Temperature Controller

The control of the temperature of the diode array was established as an operational requirement in section 1.4. Using the work of Talmi and Simpson (1980), the precision with which the temperature must be controlled during a 30 minute integration with an array giving 500 electron-hole pairs readout noise, and being operated at - 50^{o}C, is $\approx$6 mK. However their result is based on the temperature dependence of the leakage current, and so is not useful when that current is negligible as occurs with cryogenically cooled arrays. For this case of the operating temperature, critical parameters of the array, for example those causing the fixed-pattern and flat-field responses, are the quantities being stabilized. The author is unaware of any quantitative determination of the requirements for the temperature stability of those parameters. The range of precisions to which the temperatures

of some exsisting cryogenically cooled solid-state detectors are controlled, includes Campbell (1977) with $\approx 1^{o}C$, Campbell et al. (1981) with $\pm 0.2^{o}C$, Vogt et al. (1978) with $\pm 0.1^{o}C$, Vogt (1981) with with $\pm 0.05^{o}C$, and Marcus et al. (1979) with $\pm 0.01^{o}C$. Based on these, a design goal of $0.01^{o}C$ will be set for the temperature controlling precision in this detector, to ensure that the detector performance will not be adversely affected in any way by temperature instability.

The principles of a temperature controller will now be given, the techniques for applying them developed, and the controller designed and constructed. The design will be considered in a single pass through the controller, and so because the design is normally an iterative procedure, some values will be specified and used before the section occurs in which they are determined.

4.2.1 The Servo-Loop Principle

During operation of the controller, the temperature of the array mounting block, the controlled object, will be higher than the natural temperature of the block due to the controller heating the block. The controller will increase or decrease the operating temperature by increasing or decreasing the heating power it is delivering to the block. The control principle is that of a servo-loop which compares the temperature of the block to the required temperature, and if the difference is non-zero, alters the amount of heat supplied to the block so as to change the temperature to the required value.

a) Servo-Loop Theory

A servo-loop model and its analysis given by Forgan (1974) forms the basis of this section on the operating principles of a temperature controller. Figure 4.5 depicts the model as five sub-systems that are linked together in a loop by a variety of physical signals. Each sub-system has a transfer function which governs the conversion of its input signal into its output signal as

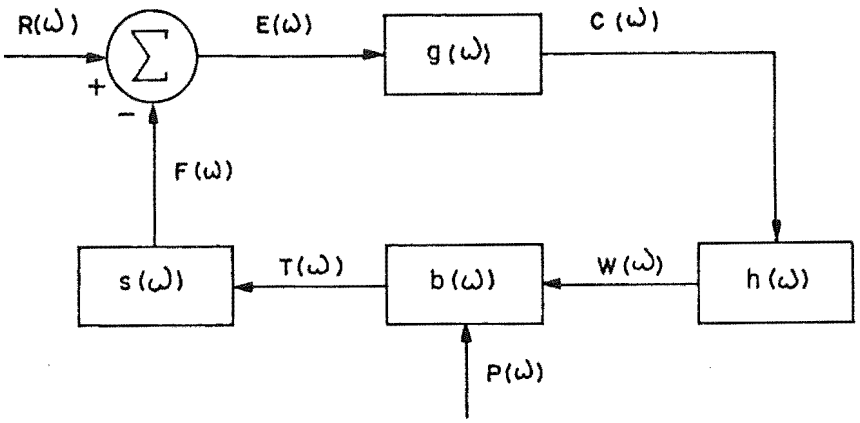


Figure 4.5: Block diagram for a servo-loop controller.

(Output Signal) = (Transfer Function)(Input Signal). (4.6)

In general, the input and output signals will have different units, and the transfer functions will be complex so as to indicate their gain and phase shift as a function of the frequency of the input signal. The temperature of the block, $T(\omega)$, is converted by the transfer function of the thermometer, $s(\omega)$, into a feedback voltage signal, $F(\omega)$. The difference between it and the reference signal voltage, $R(\omega)$, is the error voltage signal, $E(\omega)$, that indicates the deviation of the actual temperature from the required temperature. The transfer function of the amplifier in the temperature controller, $g(\omega)$, produces a correction voltage signal, $C(\omega)$, in response to that error. When the correction signal is responded to by the transfer function of the heater, $h(\omega)$, the heater supplies power $W(\omega)$ to the block. That power combined with any pertubation, $P(\omega)$, from sources external to the servo-loop, changes the temperature of the block via the transfer function of the block, $b(\omega)$. It follows that in algebraic form, the temperature of the block is

$$T(\omega) = b(\omega)[W(\omega) + P(\omega)] = b(\omega)[h(\omega)C(\omega) + P(\omega)] \ , \quad (4.7)$$

and that the correction signal is

$$C(\omega) = g(\omega)E(\omega) = g(\omega)[R(\omega) - s(\omega)T(\omega)] \ . \quad (4.8)$$

Solving for the temperature gives the servo-loop control

equation of (4.9)

$$T(\omega) = \left[\frac{b(\omega)h(\omega)g(\omega)}{1+b(\omega)h(\omega)g(\omega)s(\omega)}\right]R(\omega) + \left[\frac{b(\omega)}{1+b(\omega)h(\omega)g(\omega)s(\omega)}\right]P(\omega)$$

To make use of this equation, the functional form of the transfer functions must be determined. Excluding that subsystem referred to as the amplifier, the general function $x(\omega)$ will be assumed to be of the form

$$x(\omega) = \left[\frac{1}{1+j\omega X}\right] \qquad (4.10)$$

which is linear with an exponential response of time constant X to a step change in its input signal. It also has unit amplitude at zero frequency which implies that all the constants of proportionality are combined together in the transfer function of the amplifier. That transfer function has the functional form

$$g(\omega) = G\ a(\omega)\ , \qquad (4.11)$$

where G is the constant referred to, which must be the servo-loop gain at zero frequency, and $a(\omega)$ gives the frequency dependence of the amplifier. This amplifier must therefore also have unit amplitude when the frequency is zero so that the control equation becomes

$$T(\omega) = \left[\frac{G}{G+1}\right]R(\omega)\ . \qquad (4.12)$$

This shows that the temperature becomes that specified by the reference as the gain tends to infinity. However the control equation becomes unstable when the gain is increased to the critical gain value, G_c, the value that occurs when the denominator of that equation goes to zero at the critical frequency ω_c given by

$$b(\omega_c)h(\omega_c)g(\omega_c)s(\omega_c) = -1\ . \qquad (4.13)$$

At this gain, the system has self-sustaining temperature oscillations of frequency ω_c. The work of Nyquist as given by Forgan (1974) can be used to determine the following results regarding this instability.

1) The system is unstable at all gains above the critical gain.

2) If the time constants are well spaced in value, the critical gain is approximately the quotient of the largest and

smallest values.

3) The stability of the control equation tends to decrease as the number of time constants increases.

It follows that it is desirable for the critical gain to be as high as is possible so that a high gain value can be used to give good stabilization as indicated by equation 4.12. Therefore the value of the time constants should be well spaced in values, and the number of those constants should be minimized if possible.

b) Amplifier Types

The simplest amplifier type is called an On-Off controller because it turns the heater full 'On' if the error signal is positive, and full 'Off' if the error signal is negative. Its transfer function is therefore $g(\omega) = \infty$, having an infinite gain, $G = \infty$, at all frequencies, $a(\omega) = 1$. The temperature will therefore oscillate about the reference temperature with a peak-to-peak amplitude set by the servo-loop time constants. This amplifier type can be used if that amplitude is within the design specification for the temperature fluctuations.

Superior control can be achieved by an amplifier that manipulates the heater power to be proportional to the negative of the error signal. This amplifier type is referred to as a reverse acting proportional amplifier, and as it is the basis of the controller that has been designed for this detector, its operation will be illustrated with the schematic response curves of that implementation that are given in figure 4.6. Those curves are for a temperature of the air around the dewar of $10^{o}C$. The block transfer curve, BTC, gives the equilibrium temperature of the block as a function of the heater power, with the natural temperature, T_N, of the block occuring at zero power, and the maximum power of the heater being P_{max}. The amplifier transfer curve shows that the heater power is proportionally adjusted from 0% to 100% over a range of temperatures called the proportional band, PB, that the heater is either at 0% or 100% power for temperatures that are respectively above or below the limits of that band, and that the temperature at the centre of the proportional

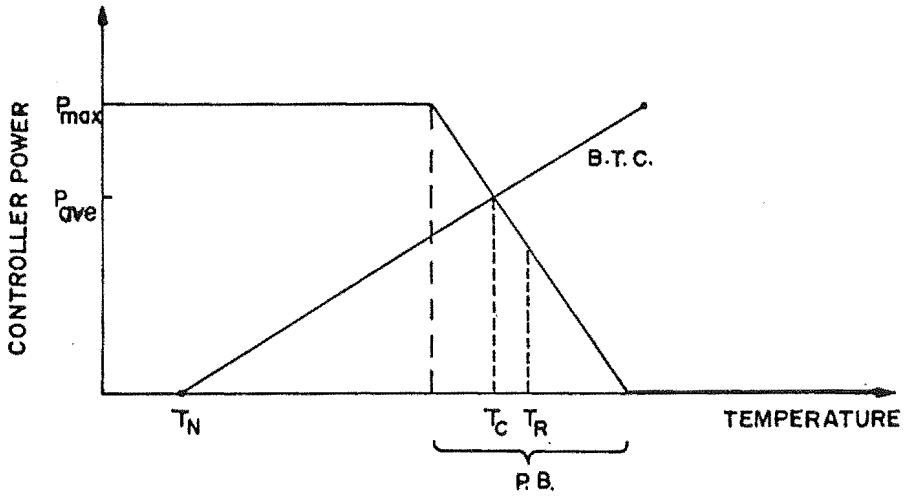


Figure 4.6: Controller power and block transfer curves as a function of temperature.

band is the control temperature, T_c. Clearly as the gain of the amplifier is increased, the width of the proportional band decreases as the gradient of the transfer curve becomes more negative. Therefore the On-Off controller is the limiting case of a proportional band of zero width. The operating temperature, T_{op}, of the controller must correspond to the intersection of the two transfer curves, and so the following properties of this type of amplifier are indicated by the position of that point.

1) The average power, P_{ave}, supplied to the block must be that required to maintain the difference between the block and natural temperatures.

2) The operating temperature will in general be different from the reference temperature, with the difference being called the temperature offset. This is because the natural temperature changes in response to air temperature changes, which results in the block transfer curve moving horizontally within figure 4.6. Thus the operating point moves along the amplifier transfer curve to effectively make the operating temperature dependent on the air temperature, with the requirement that the operating point must be within the proportional band for the temperature to be controlled. It follows that the width of the proportional band must be minimized to minimize the variations in operating temperature

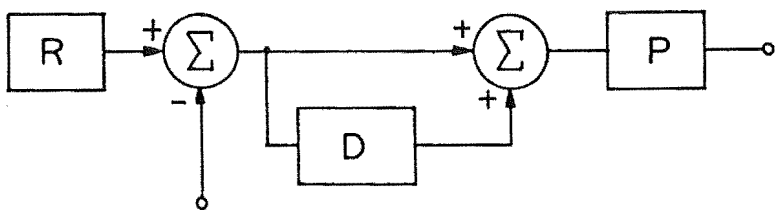
due to offset, and that the higher the heater power is, the wider is the air temperature range over which the controller will operate.

The transfer function of the ideal proportional amplifier previously described is $gp(\omega) = G$, where the frequency dependent term is $a(\omega) = 1$. This is not practicable because the infinite bandwidth of this amplifier would let an infinite amount of noise into the servo-loop from the thermometer. Therefore a real proportional amplifier includes a low-pass filter to band-limit that noise, and so has the transfer function

$$gp(\omega) = \left[\frac{G}{1+j\omega L}\right] \qquad (4.14)$$

where L is the time constant of the filter. The dynamic response of this transfer function is not the optimum one for restoring the temperature to the operating point temperature when a perturbation occurs. This is because the change in the heater power from the operating point power, which corrects the error, does not decrease to zero until the temperature is restored to the operating temperature. Because of the thermal inertia in the servo-loop, the temperature over-shoots the operating point and so will oscillate about that point with an amplitude that decays to zero as it settles with a time constant determined by the servo-loop time constants.

Superior dynamic performance can be achieved with an amplifier which before it performs noise-bandwidth limited proportional amplification, adds the derivative of the error signal to the error signal. It has the functional block diagram shown in figure 4.7, and will compensate for the rate of change of temperature to minimize the over-shoot. To



R = REFERENCE D = DIFFERENTIATOR P = PROPORTIONAL

Figure 4.7: Block diagram showing the addition of the derivative of the servo-loop error signal to that signal.

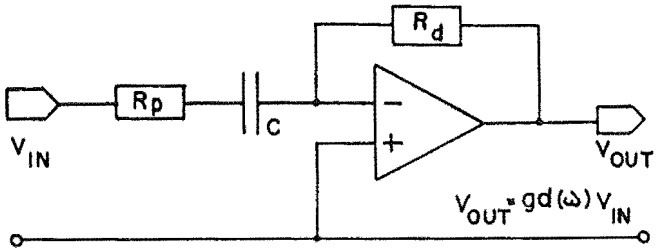


Figure 4.8: Circuit representation of a differentiating amplifier.

determine the transfer function of this proportional plus derivative amplifier, the transfer function of the differentiator shown in figure 4.8 must be determined using appendix 1 as

$$gd(\omega) = \left[\frac{R_d}{R_p+Z_c}\right] = \left[\frac{R_d}{R_p+1/(j\omega C)}\right]$$

$$= \frac{j\omega R_d C}{1+j\omega R_p C} = \frac{j\omega D}{1+j\omega P} \qquad (4.15)$$

where the differentiator time constant is $D = R_d C$, and the stabilization pole time constant is $P = R_p C$. By combining equations 4.14 and 4.15 in the way depicted in figure 4.7, the transfer function of a proportional plus derivative amplifier becomes

$$g(\omega) = gp(\omega)[1 + gd(\omega)]$$

$$= G\left[\frac{(1+j\omega[D+P])}{(1+j\omega L)(1+j\omega S)}\right] . \qquad (4.16)$$

This transfer funciton could be improved further by adding to it the integral with respect to time of the error signal. This additional signal increases or decreases the output power so that the error signal moves towards a zero value. Once equilibrium is achieved, the net integrated signal modifies the output power from the proportional plus derivative section of the amplifier by the amount required to move the proportional band so that the error signal, and therefore the temperature offset, is zero. Because the width of the proportional band is sufficiently small in the controller of this detector, integral control is not needed to reduce the temperature offset to an acceptable value.

4.2.2 Physical Realization

a) The Temperature Sensor

The temperature sensor is a diode that is operated in forward bias due to a constant current being passed through it. During that mode of operation, the potential difference across the diode is inversely dependent on the temperature of the diode. The diode used is the base-to-collecter junction of a BSY 38 transistor, which is biased with a 100 μA constant current. These diodes have been sucessfully operated at liquid helium temperatures by Smeathers (1968), and from a sample of different diodes tested in the temperature range of -196°C to 0°C by Hooker and Ritchie (1984), were found to exhibit the most linear dependence of reverse potential on temperature. The characteristics of the diode that is used in this controller have been determined for use in designing the controller.

a1) The Implementation

The circuitry with which the sensor is implemented is given in figure 4.9, and the sensor is shown in plate 5.1

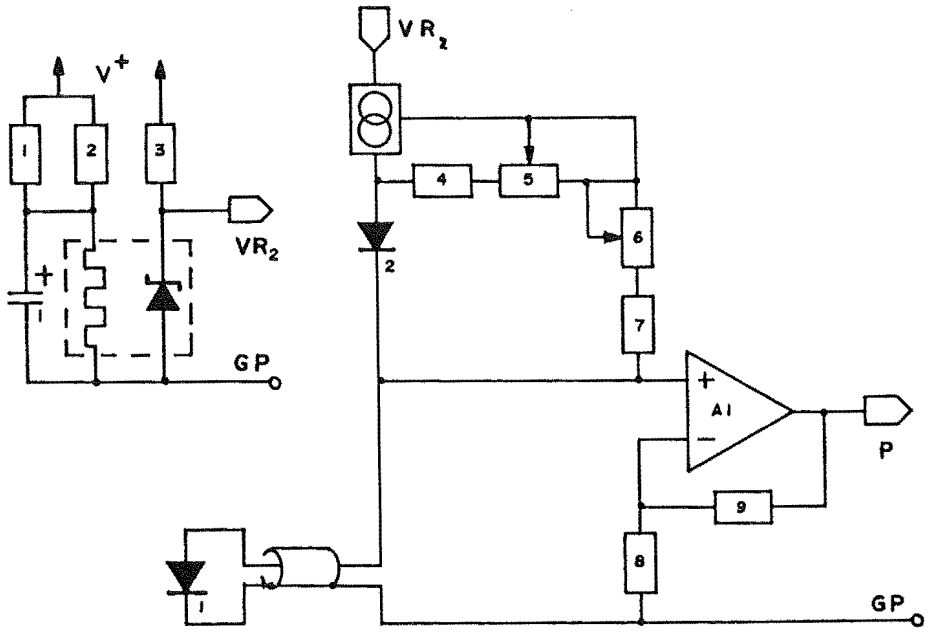


Figure 4.9: Temperature sensor electronic circuit with the precision voltage reference circuit at left.

within its mounting that is thermally connected to the block. Sensing diode 1 in its mounting is electrically insulated from the block by a mica sheet of 50 μm thickness to prevent low-frequency common-impedance coupling in the leads joining it to the amplifier. At higher frequencies, common-impedance coupling will occur through the high capacitance across that mica sheet, but will be rejected because it is outside the noise bandwidth of the servo-loop. Good thermal contact between the mounting and block is assured by the use of a thermal heat sinking compound on either side of the mica sheet.

The constant current source is an LM334 integrated circuit that is powered by the LM399 voltage reference. The source is operated in conjunction with fixed resistors 4 and 7, variable resistors 5 and 6, and diode 2. Because the temperature coefficients of the diode forward potential and the LM334 adjustment terminal to output terminal potential have different signs, the variable resistor in each of the two current sharing legs can be adjusted to achieve a zero temperature coefficient for the output current. The temperature coefficient, TC, achieved for the forward current, I_f, which is supplying the sensor is

$$TC \leq 40 \text{ ppm } (C^o)^{-1} \quad \text{at} \quad I_f = 100.0\ \mu A\ . \qquad (4.17)$$

If the constant current source is to be operated within a given range of ambient temperatures, ΔT_{ccs}, the change in the indicated sensor temperature due to the drift in the forward current is given by

$$\Delta T = \left[\frac{\Delta T_{ccs} TC}{10^6}\right] I_f \frac{dV_{bc}}{dT}\ . \qquad (4.18)$$

Using the derivatives defined in the following section , the temperature sensing error for $\Delta T_{ccs} = 20\ C^o$ is 8 mK.

a2) Physical Parameters

The time constant of the BSY 38 sensor is used in servo-loop calculations, and so has been determined from the measurement of its temperature response with time to a step change in its ambient temperature. Figure 4.10 gives such a

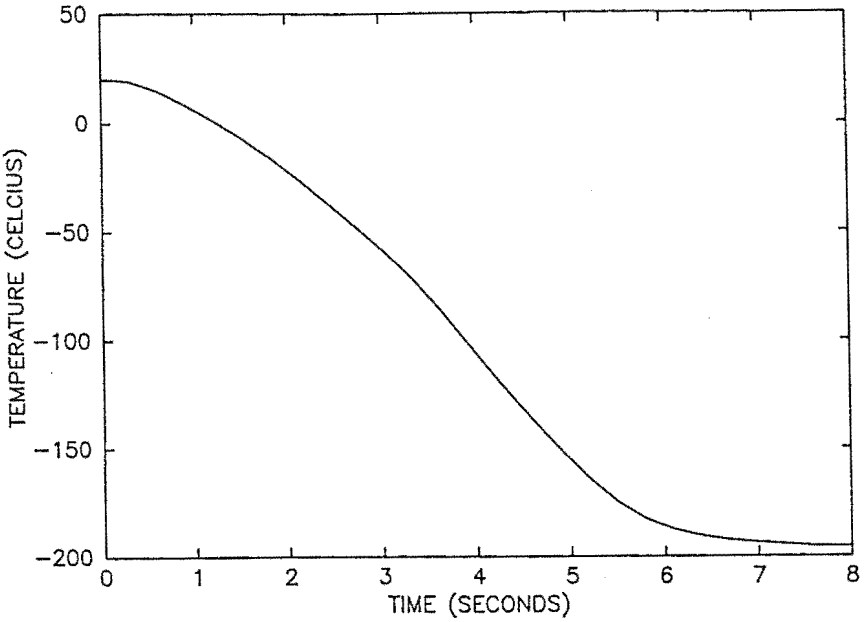


Figure 4.10: Response of a BSY 38 transistor, the temperature sensor, to immersion in liquid nitrogen.

response curve which was generated by immersing the sensor from an initial temperature of 20°C into liquid nitrogen. The time constant from that curve is taken to be

$$S = 5 \text{ seconds} . \qquad (4.19)$$

Temperatures will be determined from the response curve which gives the dependence of forward potential on temperature. This curve is assumed to be linear, and so is specified by the measured responses at the 0°C temperature of an ice-water mixture, and the -195.8°C temperature of liquid nitrogen. They are

Temperature (°C)	:	0.0	-195.8
Forward Potential (V)	:	0.579	1.023 .

It follows that the sensor response constant, the rate of change with temperature of the base to collector voltage at constant forward current, is

$$\left.\frac{dV_{bc}}{dT}\right|_{I_f=\text{const.}} = 2.265 \text{ mV K}^{-1} \quad ; \; I_f = 100 \; \mu\text{A} . \qquad (4.20)$$

A related derivative is the rate of change of forward potential with forward current at constant temperature. It is

$$\left.\frac{dV_{bc}}{dI_f}\right|_{\Delta T=const.} = 0.225 \text{ mV K}^{-1} \quad ; \quad T = -130^{o}C, \qquad (4.21)$$

and is used in specifying the required stability of the constant current source.

a3) Noise Analysis

Noise from the sensor is unavoidable, and will appear as a servo-loop error signal. That portion of it which reaches the heater will cause an undesirable equal and opposite deviation in the block temperature. It must therefore be minimized, which requires a technique to be developed for calculating the noise as a function of the parameters on which it depends. Therefore consider the noise model of the circuit diagram in figure 4.9, which is given in figure 4.11. The noise components in this figure are:

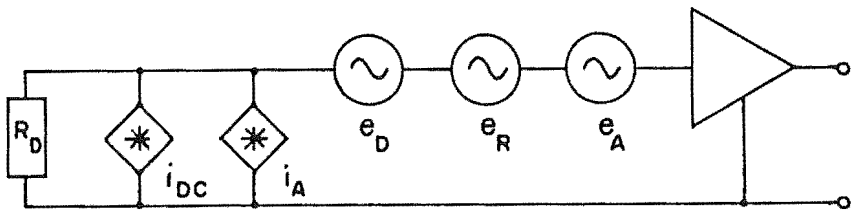


Figure 4.11: Block diagram showing the components of noise in the temperature sensor circuit.

1) R_d: the real resistance of the diode at the nominal operating temperature, which is the quotient of the forward voltage and forward current, 8.75 kΩ.

2) i_{dc}: the spectral current noise density of the forward current, which can be modelled from the noise curve in the LM334 specification sheet as

$$i_{dc} = 22\sqrt{\frac{10}{f}} \quad \text{pA}/\sqrt{\text{Hz}} \quad \text{for} \quad f \leq 10 \text{ Hz},$$

and

$$i_{dc} = 22 \quad \text{pA}/\sqrt{\text{Hz}} \quad \text{for} \quad f \geq 10 \text{ Hz}.$$

3) i_A: the spectral current noise of the amplifier input bias current, which will be ignored because the manufacturer's specifications show it to be 3 orders of magnitude smaller than i_{dc}.

4) e_D: the spectral voltage noise density of the diode resistance, which is therefore 12 nV/√Hz .

5) e_R: the spectral voltage noise density of the amplifier feedback resistors, which is therefore less than 4 nV/√Hz.

6) e_A: the spectral voltage noise density of the LF357 amplifier, which can be modelled from the noise curves in its specification sheets as

$$e_A = 12\sqrt{\frac{100}{f}} \quad \text{nV/√Hz} \quad \text{for} \quad f \leq 100 \text{ Hz},$$

and

$$e_A = 12 \quad \text{nV/√Hz} \quad \text{for} \quad f \geq 100 \text{ Hz}.$$

The current noise density appears across the diode resistance, where it exhibits a voltage noise density of

$$e_{dc} = 190\sqrt{\frac{10}{f}} \quad \text{nV/√Hz} \quad \text{for} \quad f \leq 10 \text{ Hz},$$

and

$$e_{dc} = 190 \quad \text{nV/√Hz} \quad \text{for} \quad f \geq 10 \text{ Hz}.$$

Clearly e_D, e_R, and e_A are negligible compared with this contribution to the noise, and so by ignoring them, the noise voltage density of the sensor is simply e_{dc}.

The sensor noise is bandwidth limited by the transfer function of the amplifier in the controller, and so the noise which passes into the servo-loop has an r.m.s. voltage amplitude, E_n, which is given by

$$E_n^2 = \int_{f_{low}}^{\infty} e_{dc}^2 \, |g(\omega)|^2 \, df \; . \qquad (4.22)$$

The square of the modulus of the transfer function given in equation 4.16 is too tedious to integrate, and so the integration in equation 4.22 was performed numerically with the programme BSY38NSE listed in appendix 13. The result is

$$E_n = 3.77 \quad \mu V \quad , \qquad (4.23)$$

which when divided by the sensor response contant in result 4.20, gives the r.m.s. fluctuation in the temperature due to noise of

$$T_n = 1.6 \quad mK \quad . \qquad (4.24)$$

This level of uncertainty places an unavoidable limit on the precision with which the temperature can be controlled. However that precision is acceptable for the current work, and so the sensor noise will be required to be the single dominant noise source in the servo-loop.

b) Servo-loop Design

The combination of servo-loop gain and amplifier time constants which give the optimum control must be determined so as to completely specify the servo-loop design. Section 4.2.1 established that in order to achieve precise control, the servo-loop gain should be the maximum value with which the controller can operate stably. Therefore a technique for determining the stability of the controller as a function of those parameters must be developed to enable their optimum values to be found.

b1) Theory of Stability Analysis

An inherently unstable system can appear to be stable if its parameters are set precisely to their equilibrium values, and the system is not disturbed. That state can occur because the system is static. Therefore to determine the stability of a system, it should be disturbed from its equilibrium state so that the resulting dynamic events can be observed. This can be achieved in a control system by making the reference temperature a square-wave signal whose repetition frequency, f_o, is much smaller than the critical frequency of the controller. The controller will slew the block temperature in response to each step change in the reference temperature, and the stability of the controller can then be quantified by the speed with which the new temperature is acquired to within some specified accuracy. If equation 4.9 is used with a perturbation signal of zero, the settling speed can be measured from the resulting block temperature versus time curve given by

$$T(t) = S(\omega)R(t) \ , \qquad (4.25)$$

where $R(t)$ is the reference temperature waveform, and $S(\omega)$ is the servo-loop transfer function. If the reference waveform has an amplitude of unity, it can be expressed as

$$R(t) = 0.5 + \frac{2}{\pi} \sum_{n=0}^{\infty} \frac{\sin[(2n+1)2\pi f_o t]}{2n+1} \ , \qquad (4.26)$$

and therefore the block temperature becomes

$$T(t) = \frac{S(\omega=0)}{2} + \frac{2}{\pi}\sum_{n=0}^{\infty} |S(\omega)| \frac{\sin[(2n+1)2\pi f_o t + \theta(\omega)]}{2n+1} \quad (4.27)$$

where $\omega_n = 2\pi(2n+1)f_o$, $|S(\omega_n)|$ is the transfer function modulus, and $\theta(\omega_n)$ is the phase of the transfer function.

The servo-loop transfer function can be seen in equation 4.9 to be

$$S(\omega) = \frac{b(\omega)h(\omega)g(\omega)}{1 + b(\omega)h(\omega)g(\omega)t(\omega)} . \quad (4.28)$$

Using equations 4.10 and 4.16, the denominator becomes

$$Den = 1 + \frac{G(1+j\omega[D+P])}{(1+j\omega B)(1+j\omega H)(1+j\omega L)(1+j\omega P)(1+j\omega T)} \quad (4.29)$$

and to increase stability by decreasing the number of time constants, the amplifier time constants D and P are chosen to be

$$T = D + P . \quad (4.30)$$

Therefore

$$Den = 1 + \frac{G}{(1+j\omega B)(1+j\omega H)(1+j\omega P)(1+j\omega L)} = 1 + \frac{G}{R+jI} \quad (4.31)$$

where

$$R = R(B,H,P,L) = 1 - \omega^2(BH+PL) + \omega^4(BHPL) - \omega^2(BP+HP+BL+HL),$$

and

$$I = I(B,H,P,L) = \omega(B+H+P+L) - \omega^3(BPL+HPL+BHP+BHL) . \quad (4.32)$$

Similarly, the numerator of the servo-loop transfer function

$$Num = \frac{G(1+j\omega[D+P])}{(1+j\omega B)(1+j\omega H)(1+j\omega L)(1+j\omega P)} = \frac{G(1+j\omega T)}{R+jI} . \quad (4.33)$$

Using the following substitutions,

$$X = \omega T \quad , \quad Y = G + R , \quad (4.34)$$

the servo-loop transfer function is

$$S(\omega) = G\frac{1+jX}{Y+jI} = G\frac{(1+j\omega X)(Y+j\omega I)}{Y^2 + I^2}$$

and therefore

$$S(\omega) = \frac{(Y+XI) + (XY-I)}{Y^2 + I^2} . \quad (4.35)$$

It follows that the modulus and phase of that transfer function are

$$|S(\omega)| = \frac{\sqrt{(Y+XI)^2 + (XY-I)^2}}{Y^2 + I^2} , \quad (4.36)$$

$$\theta'(\omega) = \tan^{-1}\left[\frac{XY-I}{Y+XI}\right] \quad . \qquad (4.37)$$

As the frequency increases, the quadrant, q, of the phase changes and so the actual phase is given by

$$\theta(\omega) = q(\omega)\pi + \theta'(\omega) \quad . \qquad (4.38)$$

Therefore the quadrant must be determined for each frequency, and the following method of calculation uses $q(\omega=0) = 0$ because $\theta(\omega=0) = 0$, and the result that the derivative of equation 4.37 is always negative. The method is to calculate the phase from equation 4.37 as the frequency is increased in small steps from zero up to the required frequency, and each time the phase increases in value, the running value of the quadrant is decremented.

The use of equations 4.36, 4.37, and 4.38 in equation 4.27 will give the block temperature as a function of time. This is performed by the programme TC_STP_R listed in appendix 14, to which one must give the values of B, T, H, L, D, P, F_o, and the accuracy with which the temperatures are to be calculated. The time constants are used to calculate the critical gain and frequency as a guide to the selection of G by the user. The temperature is then calculated at user specified equal increments of time within a specified range of times.

The critical parameters are determined by rewriting equation 4.13 by using parts of equation 4.31 as

$$-G_c = R + jI \quad ; \quad \omega = \omega_c . \qquad (4.39)$$

Because the critical gain is real, I must be zero at the critical frequency, and so that frequency is found from I as

$$f_c = \frac{1}{2\pi}\sqrt{\frac{B + H + P + L}{BPL + HPL + BHP + BHL}} \quad . \qquad (4.40)$$

Substituting this value into equation 4.37 gives

$$G_c = \omega_c^{\,2}(BH+BP+BL+HP+HL+PL) - \omega_c^{\,4}BHPL - 1 \quad . \qquad (4.41)$$

It follows that the servo-loop parameters can be optimized by using the curves generated with this technique to determine the stability of the controller as a function of those parameters.

b2) Servo-Loop Parameters

The block and temperature sensor time constants were determined in sections 4.1.4b and 4.2.2a respectively as

$$B = 2250 \text{ seconds, and } S = 5 \text{ seconds .}$$

However determining the heater time constant requires the non-trivial measurement of thermal power in real time. Therefore an estimate of

$$H \approx 1 \text{ second}$$

has been made based on the experience of Hooker (1984). This value is conservatively high so that if the heater time constant is the lowest in the servo-loop, a controller designed for this value will have better stability when operating with the actual value. The reason is that the critical gain, approximately the quotient of the highest and lowest servo-loop time constants, would increase. However if the actual time constant was not the lowest in the servo-loop, there would be little change from the stabiltiy calculated with the specified time constant.

The remaining time constants to be specified are the amplifier constants L, D, and P. Equation 4.30 places a constraint on D and P which increases the servo-loop stability, and according to section 4.2.2a2, they are also constrained to values which minimize the noise bandwidth through which the sensor noise passes into the servo-loop. As a result of those considerations, they have been chosen to be

$$L = 0.64 \text{ seconds, } D = 4.36 \text{ seconds, and } P = 0.64 \text{ seconds.}$$

Therefore once the required stability has been quantified, the dynamic response analysis can be performed to determine the servo-loop gain. From the consideration of dynamic response curves for a wide range of servo-loop parameters, a temperature over-shoot of between 5% and 10% for a step input in the reference temperature has been chosen. For the above parameters, this corresponds to gains between 312.5 and 350, and the conservative choice of

$$G = 312.5$$

has been made. The step response under these conditions is shown in figure 4.12, which shows that the gain is not only sufficiently high for the unavoidable temperature sensor time constant to determine the rise-time, but also sufficiently low that the controller rapidly and smoothly acquires the new temperature.

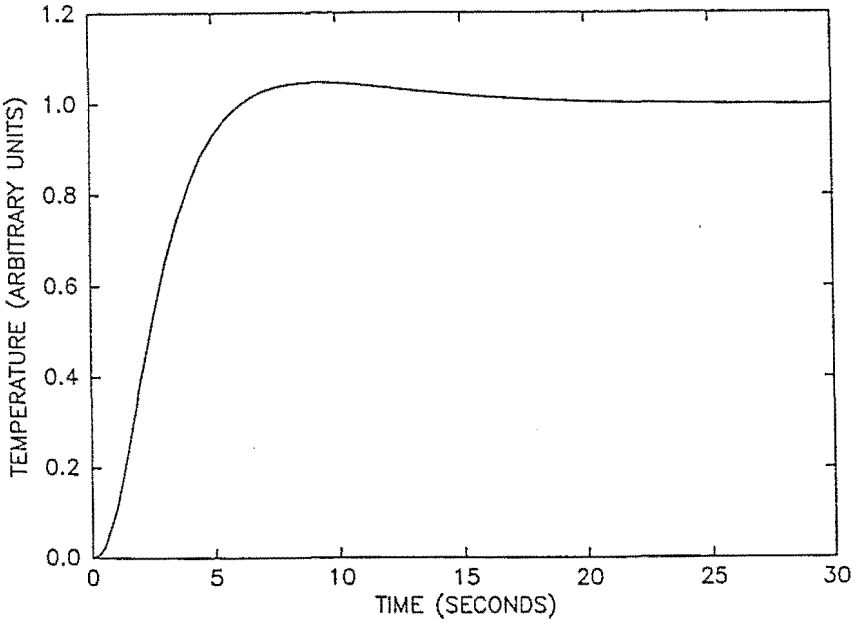


Figure 4.12: Response of the temperature controlling circuitry to a step input.

c) The Electronic Circuitry

The above servo-loop parameters now enable the physical hardware to be designed. The designs of the block and temperature sensor have already been given in sections 4.1 and 4.2.2 respectively. Therefore the heater and amplifier remain to be designed.

c1) The Heater

A design goal has been set that there should be a reference temperature at which the controller can hold the block over a dewar ambient air temperature range of $\Delta T_r = 25$ C^o. Given the thermal resistance, R_t, found for the link in

section 4.1.4, and equation 4.5, a maximum heater power of

$$H_p = \frac{\Delta T_r}{R_t} \frac{\Delta T_b}{\Delta T_a} = 1 \text{ watt} \qquad (4.42)$$

is indicated. The heater must be tightly coupled to the block to minimize its time constant, and so it is located on the heater rod. It is essentially a 100 Ω resistor across which the controller amplifier can develop a voltage of between 0 and 10 volts to dissipate a power of between 0 and 1 watt. It was physically constructed by winding a coil of enamel coated constantine wire over a sheet of tobacco paper on the rod which was wet due to being soaked in araldite glue. The paper provides additional insulation between the coil and rod, and is held on the rod during winding by the wet glue. The principal purpose of the glue is to provide a low thermal resistance contact between the coil and rod to ensure a low heater time constant. The 100 Ω length of wire was folded in half and wound onto the rod as a double strand. This non-inductive winding technique ensures that the coil does not radiate a magnetic field near the array as the heater current changes in the control process. The gauge of wire was chosen so that the length required to wind a 100 Ω resistor would form a coil of 25 mm length on the 12.5 mm diameter heater rod. This length ensures that the maximum power dissipation per unit area is kept to an acceptable value of 0.1 W cm^{-2}.

c2) The Amplifier Gain

In the formalism of the servo-loop theory in section 4.2.2b1, the combination of the transfer function amplitudes into the servo-loop gain can be expressed as

$$G = S_r R_t H_r A \quad , \qquad (4.43)$$

whose units are

$$[V/V] = [(V/K)(K/W)(W/V)(V/V)] \, ,$$

where S_r is the temperature sensor response constant, R_t is the thermal resistance of the block, H_r is the heater response constant, and A is the electronic amplifier gain. The previously found values are

$$G = 312.5 \text{ V V}^{-1}, \qquad S_r = 2.265 \text{ V K}^{-1},$$
$$R_t = 13 \text{ K W}^{-1}, \text{ and} \qquad H_r = 0.1 \text{ W V}^{-1}.$$

which implies that the electronic amplifier gain is

$$A = 115000 \text{ V V}^{-1}.$$

If the maximum output voltage from the amplifier into the heater is V_m, the width of the proportional band will be

$$\Delta T_{pb} = \frac{V_m}{S_r A} = \frac{V_m H_r R_t}{G}, \qquad (4.44)$$

and therefore $\Delta T_{pb} = 0.042$ K.

The controller will be able to operate with a proportional band of this width because the peak-to-peak sensor noise, which follows from section a3 as approximately 0.01 K, is less than the proportional band width.

c3) The Amplifier Circuit Diagram

The amplifier that has been previously specified is implemented by the circuitry shown in figure 4.13. The four amplification stages A1, A2, A3, and A4 provide the gain of A that is required from section 4.2.2c2. The gain of stage A1 is 12, which is the maximum value with which it will not saturate if the lower limit of its temperature range is the temperature of liquid nitrogen. This enables the stage to be used as the preamplifier of a block thermometer. Stage A2 forms the negative of the temperature error signal, and its gain is limited to -1.66 because the low value of the maximum available reference voltage is required to correspond to a minimum temperature limit of $\approx -145^{\circ}$C. Stages A3 and A4 each have a gain of 88, and the low-pass filter of time constant $L = R_{15}C_3$ is at the input of A4. This position ensures that the sensor noise is band-limited before it is amplified to an amplitude which would saturate the following amplifiers. Amplifier A5 is the differentiator, whose time constants are $P = R_{18}C_4$ and $D = R_{18}C_4$. The negated sum of the output of A4 and its derivative is produced by A5, and is the drive signal for the heater. Because the power dissipated by the heater is proportional to the square of the potential difference across

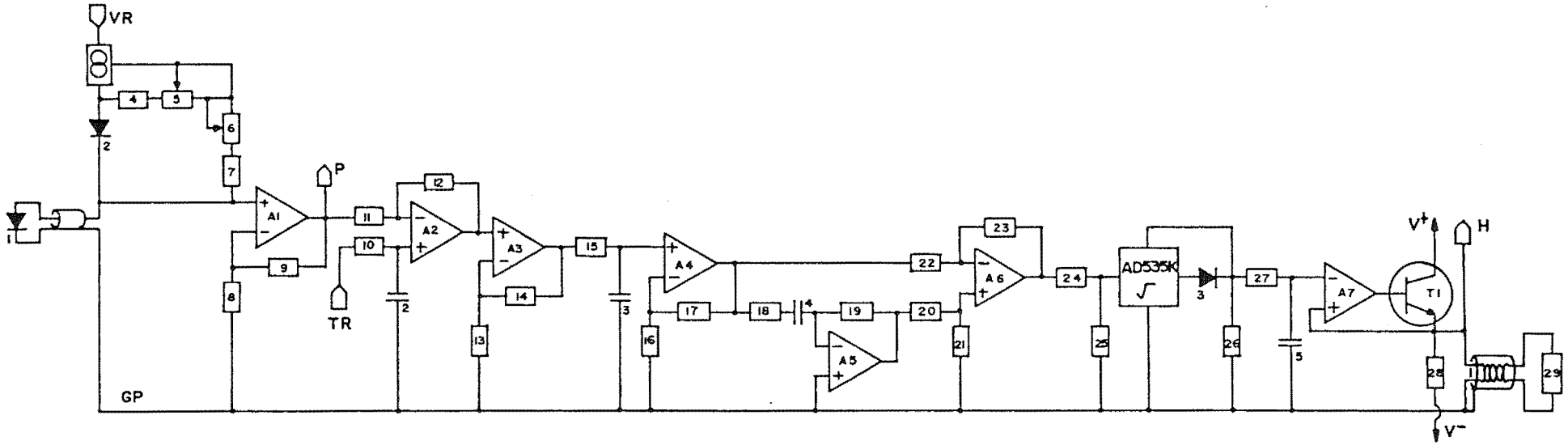


Figure 4.13: Temperature controller electronic circuit.

its resistance, the square-root of the signal from A6 is formed by the AD535K. The unity gain combination of amplifier A7 and power transistor T1 supply the current drive for applying that signal to the heater, resistor 29, where the power developed will be linearly related to the output signal of the temperature controller amplifier. Because the AD535K has a maximum input voltage of 10 volts, while the ouput of A6 can have an amplitude of up to 13.5 volts, the signal from A6 is attenuated by the factor 10/13.5 with the resistors 24 and 25. That attenuation is compensated for by the product of the gains from stages A1, A2, A3, and A4 being a factor of 1.35 higher than the required servo-loop value for A. Three additional areas of circuitry ensure that the heater is driven with the correct noise free signal. Diode 3 and resistor 26 ensure that the output voltage of the AD535K remains at zero volts when its input voltage is negative. Resistor 27 and capacitor 5 form a low-pass filter whose time constant is 1.6 milli-seconds, and which attenuates any high frequency noise coupled into the temperature controller so that it is not sent into the dewar. Resistor 28 ensures that T1 is biased with a non-zero collector-to-emitter current that is independent of the load current being supplied to the heater. This is required to ensure the transisitor remains active in the feedback mechanism to A7 when the heater voltage is zero.

The heater power signal is connected from node H to the A/D convertor input multiplexer, as shown in figure 5.13, so that its value can be displayed by the Data Acquisition System. Resistors 22, 23, and 24 are used to scale the 0 to 10 volt range of the heater power signal so that it lies within the input range of the A/D convertor.

The reference temperature used by amplifier A2 to form the error signal is one of two user selectable values generated by circuitry shown in figure 4.14. Each of those signals can be adjusted to a required value by use of the two variable resistors. Those resistors are padded with additional fixed value resistors to limit the range of adjustment to approximately $10^{o}C$. The reference voltage used is that described in section 4.2.2a1.

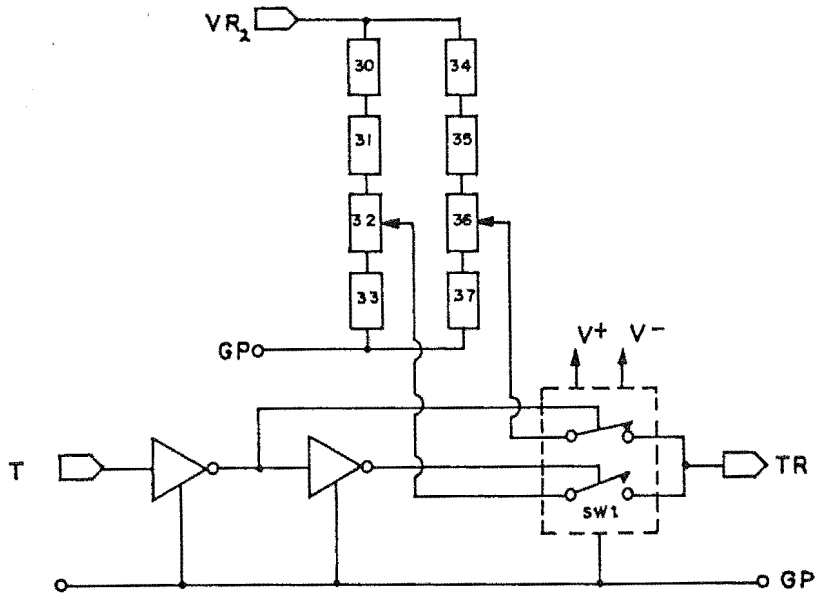


Figure 4.14: Reference temperature electronic circuit.

c4) The Printed Circuit Board

The temperature controller is situated on the printed circuit board in the A/D electronics box as specified in section 3.2.3. The controller occupies the top right corner of that board which is shown in plate 5.3, and whose layout is given in figure 5.15. The path of the signal processing starts at top centre with the sensor amplifier, and proceeds in an anti-clockwise loop around the non-polarized differentiator and low-pass filter capacitors, to finish at the power transistor. The general design techniques of the physical circuitry have been given in section 3.2.4, requiring only one additional aspect to be considered. Common-impedance coupling must be avoided between the temperature sensor and heater ground return paths which pass into the dewar from this board. This is because the maximum heater circuit current of 100 mA could produce a 0.1 mV EMI voltage in the sensor circuit, equivalent to 0.05°C, if those circuits shared as little as 1 mΩ of common ground impedance. Therefore dedicated ground returns are used for each of those components between them and the printed circuit board.

4.2.3 Performance

The precision with which the temperature of the block is controlled can be determined by observing the error signal within the servo-loop. A technique for achieving this is for the user to monitor the temperature controller power that is updated at 1 second intervals in the real-time information supplied by the LDA programme, as described in Chapter 7. The standard deviation, σ, of that signal can be found, for example, as one third of the estimated width of the error band in which five out of six samples fall. The units are fractions of the full heater power, and can be converted into a temperature because the full heater power corresponds to the width of the proportional band. It has been found that an upper limit on this standard deviation corresponds to the noise of the sensor calculated in section 4.2.2a3. This indicates that the precision of the control process is solely limited by the noise of the sensor, and that its 6σ error band is less than $0.01^{o}C$. This precision can be maintained over periods of many hours, with the long-term precision being determined by the width of the proportional band and the ambient temperature as discussed in section 4.2.1b. Additional confirmation of this result can be gained by monitoring the block thermometer, described in section 4.3.1, at the output of the A/D convertor. The least-significant-bit, LSB, size for that thermometer corresponds to 1/64th C^{o}, and that bit is not seen to toggle in digitized readings from the thermometer being made at an 8 kHz rate during periods of hundreds of seconds.

4.3 The Thermometers

4.3.1 The Block Thermometer

The temperature of the block is measured by this thermometer, and displayed in real time as described in section 7.2.1. The thermometer is designed so that its output over the maximum conceivable block temperature range of $-196^{o}C$ to $30^{o}C$ can be digitized by the system A/D convertor. Because

of the input voltage range of that convertor, the zero-point of the temperature scale corresponds to thermometer output voltage of zero, and that voltage increases as the temperature decreases.

The block temperature sensor developed in section 4.2.2 for use with the temperature controller, is also used for this thermometer. Output node 'P' in figure 4.9 is used as the input to the thermometer, whose circuitry is shown in figure 4.15. Two amplifiers are used so that the zero-point and

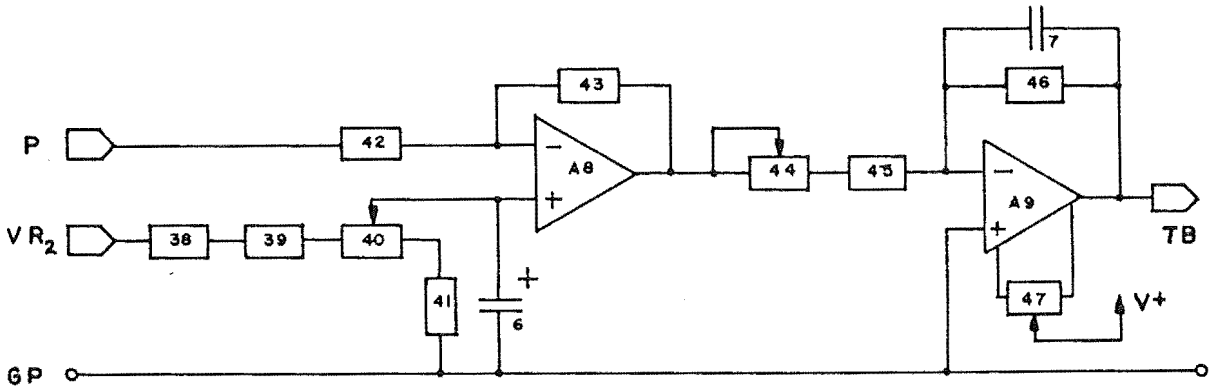


Figure 4.15: Block thermometer electronic circuit.

scale factor of the thermometer can be independent of each other. Variable resistor 40 is used to set the output voltage of amplifier A8 to 0 volts when the sensor temperature is 0 ^{o}C. Variable resistor 47 is then used to trim the input offset voltage of amplifier A9 to 0 volts so that amplifier A9 does not influence the previously set zero-point. Finally, variable resistor 44 is used to set the voltage versus temperature scale factor of the thermometer so that the A/D convertor LSB size corresponds to 1/64 C^{o}. The analogue output voltage goes to the A/D convertor input multiplexer described in section 5.5.

Sensor noise is bandwidth limited by the action of capacitor 7 combining with resistor 46 to from a low-pass filter with a 15 millisecond time constant. The r.m.s. noise can be found as described in section 4.2.2a3 if the derivative and stabilization pole time constants tend to infinity and zero respectively. That noise is approximately 1 mK, indicating that the peak-to-peak noise will be less than the

quantization in the thermometer data. Capacitor 6 prevents noise coupling to the thermometer signal through the zero-point signal that is generated from the reference voltage.

This thermometer is located along the left side of the temperature controller on the printed circuit board shown in plate 5.3, whose layout is given in figure 5.15. The techniques used for its fabrication have been given in section 3.2.4.

4.3.2 The Ambient Thermometer

The temperature of the air surrounding the dewar is measured by the ambient thermometer whose circuitry is given in figure 4.16. Its temperature sensor is an LM335 integrated

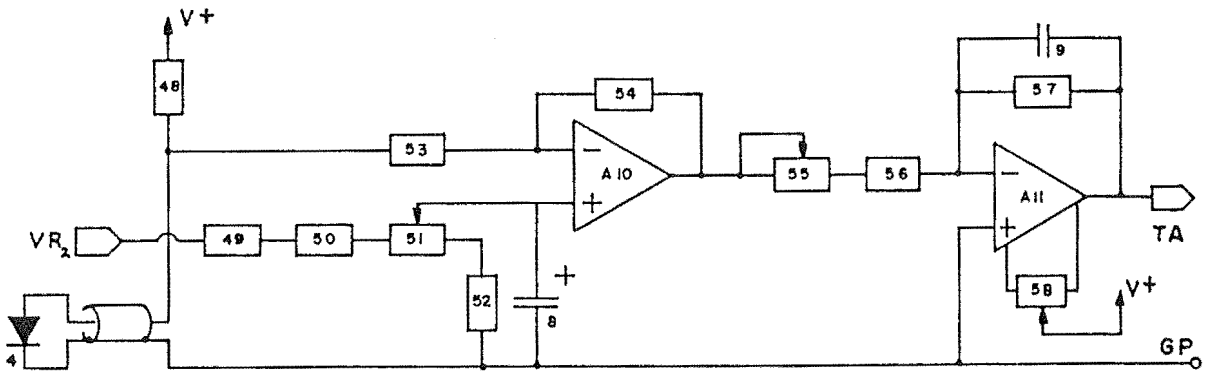


Figure 4.16: Ambient thermometer electronic circuit.

circuit which is located in the temperature equalizer shown mounted by a thermal insulating material to the top of the A/D electronics box in plate 4.1. Resistor 48 acts as a constant current source for the sensor, whose current is sufficiently constant over an ≈0.25 volt variation in the power supply voltage for the indicated temperature to vary by no more than ≈0.01°C. The remaining circuitry performs exactly as described for the block thermometer, except that the output voltage increases with increasing temperatures, and the available temperature range is ≈-30°C to +200°C. The analogue output voltage goes to the A/D convertor input multiplexer described in section 5.6.2.

This thermometer is located in the top left corner of the 'A/D and thermal control' board given in plate 5.3 and figure 5.15.

CHAPTER FIVE

VIDEO PROCESSING

The operating principles developed in Chapters 1 and 2 indicate that the video processing electronics must perform four major tasks. They must bias the diode array, then amplify the video signal, minimize its noise content, and convert it into recordable numbers. The possible readout techniques they can use for acquiring that signal were described in section 2.2, where the readout technique of video voltage level processing was selected. Given the complete framework which has been developed for the video processing electronics to operate within, the requirements for those electronics must be determined, their circuitry must be designed, and they must be explicitly fabricated.

5.1 General Design Requirements

The performance objectives for the video processing electronics must be specified in order to be used for determining the requirements of the electronic design. They initially enable the selection of a class of components capable of achieving the required performance, whose typical operating frequency determines the operating frequency of the system.

5.1.1 Performance

A design principle will be specified which requires the net signal error from each type of undesirable video processing response to be equivalent to some fraction of the readout noise, σ_r. It follows that a goal must be set for the net readout noise, which will be

$$\sigma_r \leq 500\ e^-/h\ \text{pairs} \qquad (5.1)$$

for the Reticon RL 936F/30 device to be used. The three types of undesirable responses are noise, non-linearity, and instability.

The video processing noise will be quantified as the noise measured at the output of the video processing chain when the input is a noiseless signal of the same load characteristics as the diode array. That noise will be required to contribute less than half the net readout noise power, which is equivalent to having an amplitude, ϕ_{vp}, of less than $\sigma_r/\sqrt{2}$ = 350 e^-/h pairs.

Non-linearity was discussed in section 1.1.2, and the design requirement on the non-linearity error term in the transfer function is that its peak amplitude should be less than $\frac{1}{2}\sigma_r$. This will allow it to be ignored in the transfer function correction process.

The sources of instability which will be explicitly controlled are those which produce signal level drifts that result in an additive offset to the data in fixed patterned frames. Any mechanism causing such an offset will be said to cause electronic baseline instability. In a stellar spectrum frame, this is equivalent to a shift in the continuum level which has the undesirable effect of changing spectral line equivalent widths and profiles. By controlling it to within a level of $\frac{1}{2}\sigma_r$, the unavoidable thermal leakage is the only contributor to the baseline.

5.1.2 Operating Frequency and Hardware

Section 3.1 indicates that the operating frequency of the system should be as low as is practicable to minimize the typical EMI coupling components within the system. This choice also maximizes the performance of passive components because their undesirable reactances, such as capacitance in parallel with resistors, and inductance in series with capacitors, become negligible.

The characteristic frequency of the information on a given video line can be seen in section 2.2.1 to be 2 times the frequency of the ϕ-clocks, ϕ_f. Therefore the frequency band the system operates within is approximately the decade above the frequency of those clocks. Inspection of the frequency dependence of key active component parameters, which are given in manufacturer specification sheets, shows that operational amplifiers and their related devices provide the

required noise, linearity, and stability performance at the lowest frequencies. Considering the frequencies in which their open loop phase shifts are -90^{o}, their open loop gains, common-mode rejection ratios, output impedances, and power supply rejection ratios are at best while in the frequency decade between 1 and 10 kHz. Therefore the design will be required to use those component types, and ϕ_f will be set at 1 kHz.

These choices are consistent with experience gained when using Hall's (1981) LDA development system, with Vogt's (1981) choice of components and ϕ_f = 1.25 kHz, and with Geary's (1981) proposed scheme of video processing.

5.2 Diode Array Bias Supply

The bias supply reverse biases the photo-diodes so that they operate in the charge storage mode as discussed in section 2.1.2.

5.2.1 Requirements

Percival and Nordsieck (1980) have demonstrated that the leakage current of a photo-diode is linearly dependent on the charge of the diode. Therefore the leakage rate is a function of the signal charge, which will produce non-linearity of some amplitude between diodes of different signal levels within the same spectrum. To ensure that the variation in the diode charge due to typical signals is a small fraction of the initialized diode charge, and therefore that the non-linearity is minimized, the bias supply voltage, V_b, should be a high value. A nominal value of V_b = 5 volts will be used because the array specification sheet in appendix 6 indicates that this is a high value which is safe for the device.

The amplitude of the bias supply determines the initialization charge on the diode that represents a signal of zero. Any variation in that quantity between the times of readout and initialization is indistinguishable from an equivalent signal charge, and is therefore a baseline shift. It follows from equation 5.4 that the maximum allowed baseline

shift of $\frac{1}{2}\sigma_r$ will occur for a 62 μV variation in the bias supply. That variation can be due to thermal drift and noise. In the case of thermal drift, if a $\approx$ 4 C^o change in the ambient temperature of the bias supply is to be tolerated during an integration, the temperature coefficient, TC, for the nominal supply voltage of 5 volts is required to be $TC_{bias} \approx 3$ ppm $(C^o)^{-1}$. In the case of noise, if the longest integration is to be $2x10^4$ seconds, the bias supply noise amplitude is required to be less than 62 μV in the frequency band which has a lower limit of $f_{bias,low} = 5x10^{-5}$ hertz.

The bias supply is in series with the video line, and so its noise is an unattenuated input signal for the video processing electronics. Therefore the bias supply noise level must also meet the requirements of the readout noise within the bandwidth of the video processing electronics.

5.2.2 The Circuitry and Implementation

The circuitry for the bias supply is shown in figure 5.1. The required voltage level is generated from the video processing precision voltage reference shown in figure 5.6, by the resistor divider network inclusive of resistors 1 and 11. Those resistors have positive temperature coefficients of less than 5 ppm $(C^o)^{-1}$. The noise of the reference and divider resistors is filtered by the RC circuit formed by the output

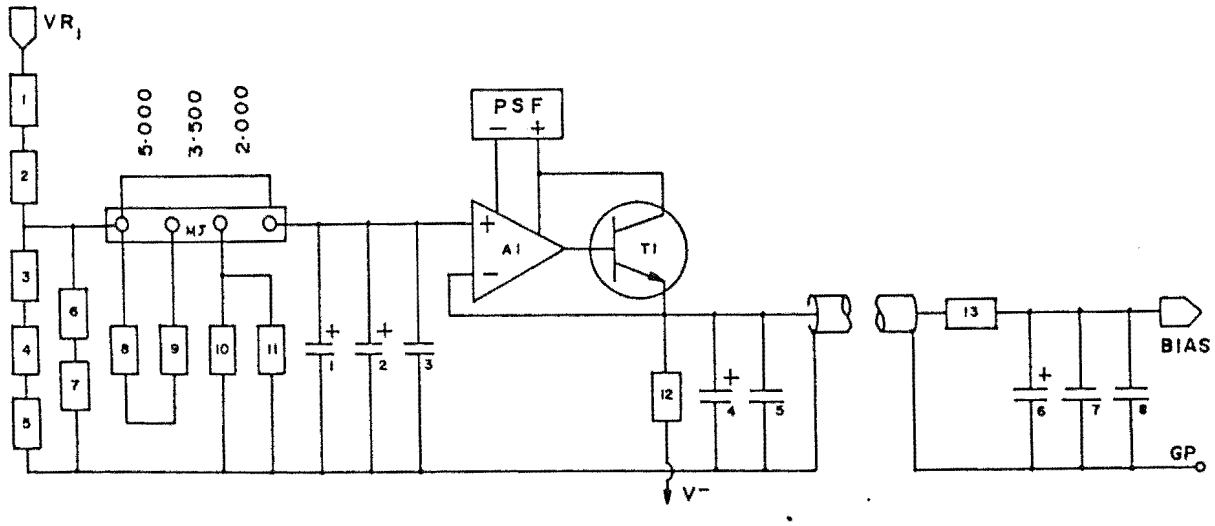


Figure 5.1: Electronic circuit for the LDA bias supply.

resistance of the divider, $R_{o,div} \approx 15$ kΩ, and the capacitors 1 to 3. They set a noise bandwidth of 0.7 Hz, which will make that source of noise negligible in the video processing bandwidth. Two 10 μF tantalum capacitors are used because they can achieve the required capacitance with a leakage current temperature variation which will not contribute to TC_{bias} for the given value of $R_{o,div}$.

The conditioned reference voltage is buffered by amplifer A1, which uses the medium power transistor T1 and capacitors 4 and 5 to generate the supply with a low output impedance. Resistor 12 ensures that the transistor is biased on for zero current loads, and for any positive output voltage.

The supply is passed through the flange to the preamplifier board where it feeds two RC filters, which in turn supply the two shift registers. Each filter has resistor 13 and capacitors 6 to 8 which form a noise bandwidth of 34 Hz to filter the amplifier noise, and any EMI from the distribution path. It is possible to have the series resistor 13 in the supply because the dc load current is zero. The AC current drawn by the array when reading out is supplied by the capacitors 6 to 8, which have an impedance to ground of less than 100 mΩ for all frequencies from the lowest system frequency of 1 kHz, to an upper frequency of 20 MHz. The location of the capactiors near to the array ensures that the zero signal reference of the bias supply is the same as that of the array.

The three position mini-jump in the divider network allows rapid selection of one of the three possible output voltages 5.00 volts, 3.50 volts, and 2.00 volts. The results of Percival and Nordsieck (1980) show that the lower value choices will allow the array to be operated at higher temperatures for a given leakage rate thermal leakage current. This will enhance the RQE for observations at wavelengths greater than 10,000 Å.

The bias supply is located in the top centre of the Video Processing printed circuit board, whose layout is given in figure 5.8, and which is shown in plate 5.2. Its output filter is located at the bottom of the preamplifier board which is similarly given in figure 5.4 and plate 5.1.

5.2.3 Performance

Using the results of appendix 5 and the divider resistor temperature coefficients, the temperature coefficient of the divider output voltage is determined to be ±2.5 ppm $(C^o)^{-1}$ when the ±1 ppm $(C^o)^{-1}$ coefficent of the reference voltage is included. This is combined with the 5 μV $(C^o)^{-1}$ input offset voltage drift of the amplifier, which is equivalent to a ±1 ppm $(C^o)^{-1}$ temperture coefficient, to give the bias supply temperature coefficent of

$$TC_{bias} = 3.5 \text{ ppm } (C^o)^{-1} . \qquad (5.2)$$

The noise in the video processing bandwidth is entirely from the amplifier because at those frequencies, the divider RC filter has attenuated the reference and divider noise by more than 60 dB. The amplifier spectral voltage noise of 12 nV/√Hz is attenuated by the bias supply RC filter. The attenuation becomes a constant 40 dB above 3.4 kHz, the frequency at which the capacitors become self inductive, and remains at that level up to a frequency of 20 MHz. The bias supply spectral voltage noise is therefore

$$e_{bias} \leq 0.4 \text{ nV/}\sqrt{\text{Hz}} \quad ; \; 1 \text{ kHz} < f < 20 \text{ MHz}, \qquad (5.3)$$

which includes the video processing bandwidth.

Within the bandwidth set by the duration of an observation, the net noise of the bias supply originates from the precision reference and the amplifier. For the reference, the noise between $f_{low,bias}$ and the divider noise bandwidth limit can be deduced from the manufacturer's specifications to be less than 1 μV r.m.s. The low frequency spectral noise density of the LF 356 amplifier used was modelled in section 4.2.2a2, and when integrated, gives the noise of the amplifier within the 50 Hz noise bandwidth of the bias supply as $\approx$ 0.4 μV. Defining the amplitude of the noise as six times its standard deviation, the amplitude of the combined reference and amplifier noise is $\approx$ 6μV, approximately 10 % of the maximum allowed value.

5.3 Video Amplification

To obtain maximum sensitivity from the detector, the video signal level equivalent to σ_r must be resolved by the A/D convertor. Therefore the video processing electronics must contain an amplification process to scale the video signal to the appropriate level.

5.3.1 Video Processing Gain

The net gain of the video processing chain, G_{vp}, will be calculated as the quotient of the required σ_r equivalent voltage at the A/D convertor, $\Delta V_{A/D,\sigma}$, and the σ_r equivalent voltage on the video line, $\Delta V_{v,\sigma}$. Therefore those voltages must now be calculated.

The A/D convertor to be described in section 5.6 will resolve its full scale input voltage range, $\Delta V_{A/D,fs} = 10$ volts, into a 14-bit binary word. It achieves the accuracy required of the conversion process with $\sigma_r \equiv 3$ LSBs or more, and so the lower limit is chosen to maximize the dynamic range of the detector. Therefore the σ_r equivalent signal at its input is

$$\Delta V_{A/D,\sigma} = \left[\frac{3}{2^{14}}\right] \Delta V_{A/D,fs} \quad . \tag{5.4}$$

The specification sheet for the diode array, reproduced in appendix 6, gives the saturation charge for a diode as

$$q_{sat} = 3.2 \text{ pC} \equiv 20 \text{ M } e^-/h \text{ pairs} \tag{5.5}$$

when the bias voltage is $V_b = 5$ volts. It follows that the photo-diode capacitance is

$$C_d = 0.64 \text{ pF} \quad . \tag{5.6}$$

The video line capacitance is also given as 33 pF, and so allowing 7 pF for the amplifier and external video line capacitance, the net video line capacitance is

$$C_v = 40 \text{ pF} \quad . \tag{5.7}$$

With these results, equation 2.8 gives the video voltage signal for a saturated diode as

$$\Delta V_{v,sat} = \left[\frac{C_d}{C_d+C_v}\right] V_b \approx 79 \text{ mV} , \qquad (5.8)$$

which corresponds to the actual measured value. This result can be used to write the σ_r equivalent signal on the video line as

$$\Delta V_{v,\sigma} = \left[\frac{\sigma_r}{q_{sat}}\right] \Delta V_{v,sat} \approx 2.0 \ \mu V . \qquad (5.9)$$

Therefore it follows that the net video processing gain will be required to be

$$G_{vp} = \frac{\Delta V_{A/D,\sigma}}{\Delta V_{v,\sigma}} = \left[\frac{3}{2^{14}}\right]\left[\frac{\Delta V_{A/D,fs}}{\Delta V_{v,sat}}\right]\left[\frac{q_{sat}}{\sigma_r}\right] = 930 \text{ V V}^{-1}. \qquad (5.10)$$

These results can be used to determine three additional parameters which are useful for describing the system.

The signal charge which corresponds to the full scale signal at the A/D convertor is

$$q_{A/D,fs} = \left[\frac{2^{14}}{3}\right]\sigma_r = 2.73 \text{ M e}^-/\text{h pairs}, \qquad (5.11)$$

the video line signal corresponding to the full scale signal at the A/D is

$$\Delta V_{v,fs} = \left[\frac{q_{A/D,fs}}{q_{sat}}\right]\Delta V_{v,sat} = 10.75 \text{ mV}, \qquad (5.12)$$

and the equivalent signal charge of an A/D convertor LSB is

$$q_{LSB} = 167 \text{ e}^-/\text{h pairs}. \qquad (5.13)$$

5.3.2 Preamplification

The first signal processing component of video voltage level processing is the high input impedance amplifier discussed in section 2.2.1. Its primary purpose is to buffer the charge signal on the video line, effectively lowering the video line impedance to ground from ≈1 TΩ at its input, to ≈100 mΩ at its output. That process represents the charge signal as a voltage level for subsequent amplification, and while in some implementations it is also used to provide gain, it is called preamplification.

Consideration of section 3.1.1 indicates that to minimze electrostatic coupling to the high impedance video lines, the preamplifiers should be as close as is practical to

the array. Therefore they will be situated within the dewar on the printed circuit board seen attached to the cold block in figure 4.1.

a) Requirements

a1) Amplification

The preamplified signal must be transmitted from the dewar to the subsequent video processing electronics, and therefore the preamplifiers should provide sufficient gain to ensure that the amplitude of the σ_r equivalent signal level is significantly higher than the level of EMI in the transmission path. Therefore to optimize, the maximum gain that can be implemented within the available space is used. An upper limit is set for this gain by the video reset offset described in section 2.2.1a, which will be quantified in section 5.3.2c as V_r = -50 mV. Consideration of section 2.2.1b shows that this level is the lowest reached on the video line, and so after preamplification, is also the most negative output from the preamplifiers. The output level must not exceed the amplifier negative saturation level, which was set in section 3.2.4 as $V_{A,sat}$ = -12.5 volts for this system, and therefore the upper limit for the preamplifier gain is

$$G_{pa,max} = \frac{V_{A,sat}}{V_r} = 250 \text{ V V}^{-1}. \qquad (5.14)$$

A variation in the video processing gain between reading out an image and its subsequent fixed-pattern frame will introduce noise, and can result in baseline instability in the difference of those frames. The baseline instability results from the variation between the component in the frames which is due to the amplified level of the video reset offset. The noise results because the fixed pattern component in each of the frames will have a different scale. Using result 5.11 and the amplitude of the fixed pattern for a typical diode, given by Vogt et al. (1978) as 250,000 e^-/h pairs, it follows that the gain variation must be less than 1000 ppm if the variation in the fixed pattern for that diode is to be less than $\frac{1}{2}\sigma_r$. There are two possible sources for a variation in the gain of an amplifier.

The first source is the temperature coefficients of the feedback resistors, which result in the temperature coefficient for the gain, TC(G), quantified by equation A5.8 in appendix 5. It shows that the resistors must be chosen with low temperature coefficients of the same sign.

The second source results from the temperature dependence of the open loop gain, A_{vo}, of the amplifier. The closed loop gain of a non-inverting amplifier is given by Stout and Kaufman (1976) in terms of A_{vo}, the open loop phase shift, ϕ_o, and the ideal-case closed loop gain, G, determined from the resistor values, as

$$A_{vc} = \frac{G}{1 + \frac{G}{A_{vo}}} \quad ; \phi_o = 0^o \ , \tag{5.15}$$

and

$$A_{vc} = \frac{G}{\sqrt{1+\left[G/A_{vo}\right]^2}} \quad ; \phi_o = 90^o \ . \tag{5.16}$$

Table 5.1 uses those results to give the fractional error in A_{vc} as a funtion of the quotient A_{vo}/G for each of the cases.

TABLE 5.1 Amplifier fractional gain error as a function of open to closed loop gain ratio.

$\frac{A_{vc}}{G}$	error (ϕ_o=0°)	error (ϕ_o=90°)
10^0	-0.50	-0.33
10^1	-0.09	-6×10^{-3}
10^2	10^{-2}	-6×10^{-5}
10^3	10^{-3}	-5×10^{-7}
10^4	10^{-4}	-5×10^{-9}

The specification sheets for operational amplifiers made by leading manufacturers shows that A_{vo} will vary by more than one order of magnitude over the operating temperature range of the amplifier. Therefore inspection of table 5.1 indicates that the temperature coefficient of A_{vc} will be unacceptable if A_{vo}/G is too low for the value of ϕ_o in the frequency range of interest. It also follows that it is desirable for the amplifier to have $\phi_o = 90^o$.

a2) Amplifier Noise

In section 5.1.1, the net input noise of the video processing electronics was required to be $\sigma_{vp} \leq 350$ e^-/h pairs. That noise will be contributed to by the formal equivalent voltage and current noise sources of the components, by their excess noise mechanisms, and by EMI. As a design principle, the contribution which is from the component sources will be required to be less than half the noise power of σ_{vp}, or $\sigma_{c,vp} \leq 250$ e^-/h pairs. Therefore the noise from excess mechanisms and EMI is also allowed to contribute up to half of the net noise power, with $\sigma_{e,vp} \leq 250$ e^-/h pairs.

Section 5.1.2 indicates that this noise performance is required for a typical bandwidth of $\Delta f_{bw} \approx 10$ kHz. By using equation 5.9 to convert $\sigma_{c,vp}$ to an equivalent voltage, it therefore follows that the maximum input spectral density that the component noise can have is

$$e_{c,vp} = \left[\frac{\sigma_{c,vp}}{q_{sat}}\right]\left[\frac{\Delta V_{v,sat}}{\sqrt{\Delta f_{BW}}}\right] \approx 10 \text{ nV}/\sqrt{\text{Hz}} \ . \qquad (5.17)$$

The component noise of the video processing electronics can be determined from their noise model in figure 5.2 in terms of the individual noise source contributions. This figure explicitly shows the preamplifier and reset switch, combines the remaining video processing electronics into the one component, VP, and models the diode array video line impedance to ground as the video capacitance, C_v, in parallel with the video line leakage resistance, R_v. The three possible input voltage noise sources are shown, which are the

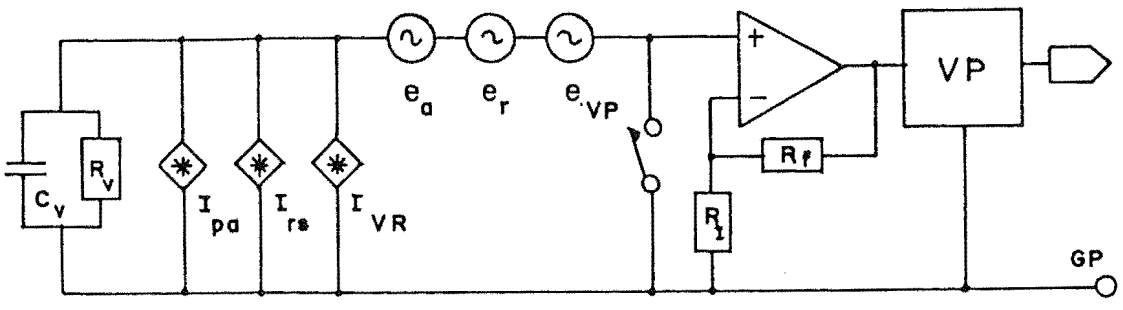


Figure 5.2: The video processing noise model.

amplifier input noise, e_a, the thermal noise (see appendix 2) of the feedback resistors, e_f, and the net voltage noise of the remaining video processing electronics when considered as an equivalent input signal, e_{vp}. Additionally, the three possible electronic current noise sources are shown, which are the amplifier bias current noise, I_{pa}, the leakage current noise of the reset switch, I_{rs}, and the equivalent noise current (see appendix 2) of the video resistance, I_{vr}. They can be combined so as to express the component spectral voltage noise density as

$$e_{c,vp}^2 = e_{v,vp}^2 + e_{i,vp}^2 , \qquad (5.18)$$

where $e_{v,vp}$ is the contribution from the voltage sources, and $e_{i,vp}$ is the voltage equivalent contribution from the current sources. Those two terms are explicitly given as

$$e_{v,vp}^2 = e_a^2 + e_r^2 + e_{vp}^2 , \qquad (5.19)$$

and

$$e_{i,vp}^2 = Z_v^2\left[I_{pa}^2 + I_{rs}^2 + I_{vr}^2\right] , \qquad (5.20)$$

where Z_v is the video impedance to ground which is seen to be

$$Z_v(\omega) = \frac{R_v}{1 + j\omega R_v C_v} . \qquad (5.21)$$

Because Z_v has a frequency dependence, $e_{i,vp}$ will dominate $e_{c,vp}$ at low frequencies, and $e_{v,vp}$ will dominate at high frequencies. To determine the significance of $e_{v,vp}$ and $e_{i,vp}$ in the video signal bandwith, consider the noise amplitude due to $e_{i,vp}$ in a bandwidth between low and high frequency limits of f_l and f_h respectively. It is found from the integral

$$E_{i,vp}^2 = \int_{f_l}^{f_h} i_v^2 |Z_v(f)|^2 df , \qquad (5.22)$$

where i_v is the net video current spectral noise density, to be

$$E_{i,vp}^2 = \frac{i_n^2 R_v^2}{2\pi C_v}\left[\tan^{-1}(2\pi R_v C_v f_h) - \tan^{-1}(2\pi R_v C_v f_l)\right] . \qquad (5.23)$$

This expression can be evaluated using the video capacitance in result 5.7, a low valued guess for the video resistance, which minimizes equation 5.23, of $R_v \approx 1$ TΩ, and the actual

value of i_v for this detector system which is given by result 5.30. The maximum possible noise amplitude results from $f_l = 0$ and $f_h = \infty$, and is

$$E_{i,vp} \approx 160\ \mu V \equiv 40{,}000\ e^-/h\ pairs\ ,\ 0 \leq f < \infty\ . \quad (5.24)$$

While the result from this frequency range is unacceptable, the result if the lower frequency limit is raised to $f_l = 100$ Hz is

$$E_{i,vp} \approx 0.8\ \mu V \equiv 200\ e^-/h\ pairs\ ,\ 10^2 \leq f(Hz) \leq \infty\ , \quad (5.25)$$

and is within the design limits. Comparison of results 5.24 and 5.25 indicate that the noise is almost entirely below the video bandwidth, which is approximately 1 kHz to 10 kHz. Therefore it follows that if cancellation techniques can be used to reject the current noise at low frequencies, while retaining the signal in the video bandwidth, the only term that contributes to $e_{c,vp}$ in equation 5.18 is $e_{v,vp}$.

Assuming the use of a cancellation technique as described above, result 5.17 requires $e_{v,vp}$ to be less than 10 nV/$\sqrt{}$Hz. The video processing term in equation 5.19 can be made negligible if the preamplifier has a sufficiently high gain. This is because e_{vp}, the video processing noise referred to the video line, is the quotient of the input noise of the video processing unit, VP, and the gain of the preamplifier. Also, the feedback resistor noise, e_r, is the thermal noise of the net resistance to ground at the inverting terminal of the preamplifier. That resistance is the parallel combination of the input and output resistances, R_i and R_f respectively, which should be less than $\approx$250 Ω so that e_r can be neglected through being less than $\approx$2 nV/$\sqrt{}$Hz. Therefore the single significant contributor to the component noise of the video processing chain is the input voltage noise of the preamplifier, and a design value of $\approx$8 nV/$\sqrt{}$Hz will satisfy the noise requirements.

a3) Video Current Deleterious Effects

The bias current of the preamplifier and the leakage current of the reset switch are the primary contributors to the undesirable current onto the video line, i_v, whose noise was considered in the previous section. A time rate of change

in the video voltage of i_v/C_v is the other significant consequence of that current. The resulting signal is required to be sufficiently stable that it does not contribute to the readout noise, and that it is a fully tractible component of the fixed pattern.

b) Existing Design

Low noise high input impedance amplifiers, of the type discussed by Maxwell (1977), can be used with negative feedback to achieve a higher input impedance and more stable gain as described by Motchenbacher and Fitchen (1973). Geary (1979) has used an amplifier of this type in his photon-counting Reticon detector, and has suggested it for use as the preamplifiers in direct imaging applications. Subsequently, Vogt (1981) has used amplifiers of this type in such a system at Lick Observatory.

Because of the use of a JFET at the input of this amplifier, it readily meets the input impedance requirements of a voltage level processing preamplifier. On first examination, it also appears to readily meet the component noise requirements determined in section 5.3.2a2 above with a typical voltage spectral noise density of ≈3.5 nV/√Hz.

The open loop gains of those amplifiers can be found by using, for example, the general results of Maxwell (1977) to be approximately 1100 V V^{-1}, and 200 V V^{-1} respectively. The corresponding open loop to closed loop gain ratios are then found to be ≈11:1 and ≈6:1 respectively. Given that these amplifiers have open loop phase shifts of $\phi_o = 0^o$, consideration of section 5.3.2.a1 indicates that the temperature coefficient of their closed loop gains will be sufficiently high that noise in flat-field frames, in excess of the formal component noise may result. One factor in the open loop gain of Vogt's preamplifiers being so low is that he has omitted the dc bias network connected at the source of the JFET in Geary's implementation.

Vogt (1982) has pointed out that the 220 kΩ resistance connected by Geary to the non-inverting terminal of the operational amplifier in his design, which compensates for the offset voltage due to the bias current of that amplifier, is

in fact a noise source which perform no useful function. An analysis of the noise contribution from that resistor indicates that it more than doubles the net noise power of the amplifier.

The active amplifier in this design is ac coupled due to the capacitor coupling the JFET stage to the operational amplifier stage. As a natural consequence, the equilbrium output voltage is zero, and the response to a step input is a step output which then exponentially decays to zero. It follows that the video signal of a given diode is expected to decay towards zero with a rate of change of voltage that is proportional to the net video level immediately after the diode is accessed. This level is equal to the sum of the diode signal and the video level at the time the diode is accessed. Therefore the net change in the video voltage during the time interval in which a given diode is being processed, is also proportional to the video signal that exists at the time the diode is accessed. That signal is a function of the previous input signals to the preamplifier, and so the net change in the diode signal, due to the exponential decay, will vary as the video signal evolves.

If the variation in the net change from the decay, due to the preceeding input signl, is larger than the readout noise, it follows that the signal will be corrupted. Because the variation is proportional to the signal size, the behaviour of the detector will still be linear in the formal sense. However it can be seen that in the simple case of two flat-field frames of different signal levels, that the quotient will have a residual pattern. Therefore this signal-level dependent behaviour is referred to as differential non-linearity.

Vogt (1981) finds that his detector is linear, but does not investigate differential non-linearity. However Campbell et al. (1981) have reported differential non-linearity, but do not indicate their type of preamplifier.

An extensive attempt to find a combination of components which would negate these problems concluded that it is not possible to do so. Therefore alternative preamplifier circuitry will be developed in the following section.

Subsequent to the construction of the alternative, a new design was developed from the design that has been discussed above. It uses additional active circuitry and significantly different component values to completely negate the above problems, and so will be the subject of a future publication.

c) The Pre-amplifier Circuit Design

The approach to the preamplifier will be one of presenting the design and its parameters, and demonstrating that they satisfy the requirement that have been previously determined. The circuitry for the preamplifier that has been implemented is shown in figure 5.3.

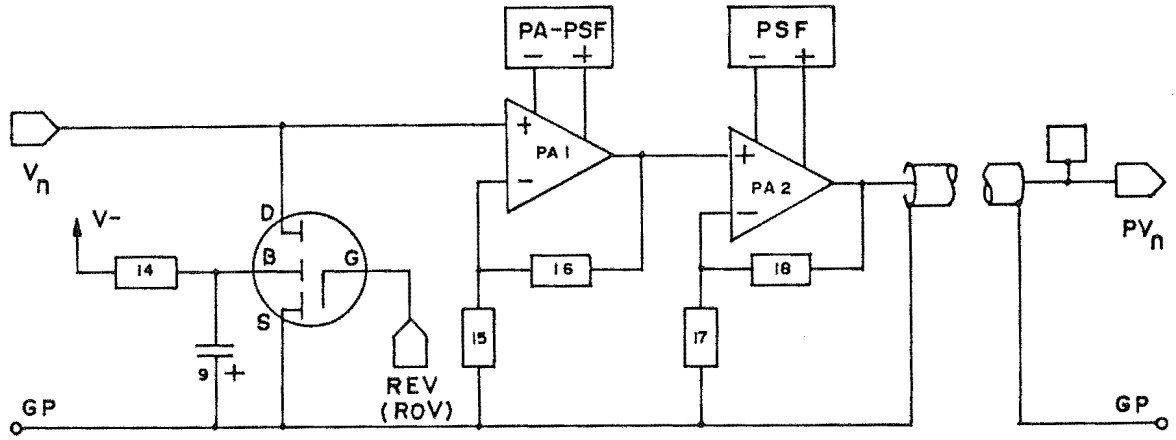


Figure 5.3: Preamplifier electronic circuit.

The preamplifier uses an SD214 D-MOS reset switch because their gate-to-drain capacitance of

$$C_{gd} = 0.3 \text{ pF} \qquad (5.26)$$

is the lowest that is available by a substantial margin, and therefore results in the lowest video reset offset voltage. It is controlled by the signal ROV (reset odd videos) when applied to video lines 1 and 2 because they have the odd numbered pairs of diodes. Similarly it is called REV (reset even videos) when applied to video lines 3 and 4 because they have the even numbered pairs of diodes. The amplitude of REV and ROV are both

$$\Delta V_{rp} = 5 \text{ volts} , \qquad (5.27)$$

because this standard logic voltage gives an adequately low 'On' switch resistance of $R_{sw} \leq 100\Omega$. Therefore the time constant for resetting the video capacitance is $\tau_r = R_{sw}C_d = 4ns$, and so to ensure that the reset operation is complete, a width for the reset pulse of $150\tau_r = 600$ ns is used.

Using results 5.7, 5.27, and allowing 0.1 pf of stray capacitance between the gate and drain, the reset video offset voltage can be evaluated from equation 2.5 as

$$V_r = -50 \text{ mV} . \qquad (5.28)$$

The base (substrate) voltage of the reset switch is held at -15 volts to minimize the leakage current onto the video line. Noise on that supply which could couple through the base-to-drain capacitance to the video line, is filtered from the video bandwidth with resistor 14 and capacitor 9. Their pole frequency is 100 Hz.

The preamplifier itself is composed of two stages of amplification. The first stage, PA1, is a Burr-Brown OPA102BM operational amplifier whose specification sheet is reproduced in appendix 7 for reference. Properties specified below for this amplifier are those which apply at frequencies within the video bandwidth.

The closed loop gain that has been implemented is $G_{pa} = 41$ V V^{-1} (32 dB). It can be deduced from the specification sheet that this is the largest value that can be used with the open loop phase shift of $\phi_0 = 90^o$, for which the quotient A_{vc}/G_{pa} is greater than 100. Therefore it can be determined from table 5.1 that the maximum possible variation in G_{pa} is 1 part in 20,000, which is within the requirement determined within section a1.

The input noise spectral density is typically $e_a = 8$ nV/$\sqrt{\text{Hz}}$, which is better than that required by result a2. Resistors 15 and 16 are respectively 300Ω and 12 kΩ, and so the thermal noise of their parallel resistance is $e_r = 2.3$ nV/$\sqrt{\text{Hz}}$. It will be shown below that the total video processing noise referred to the output of this amplifier is less than 20 nV/$\sqrt{\text{Hz}}$, and so that when referred to its input, by dividing by G_{pa1}, is less than 0.5 nV/$\sqrt{\text{Hz}}$. Therefore the net component noise is

$$\sigma_{c,vp} = 8.5 \text{ nV}/\sqrt{\text{Hz}} . \qquad (5.29)$$

The second stage of the preamplifier, PA2, is a LF357H operational amplifier that is operated with a gain $G_{pa2} = 6$. It follows that the net preamplifier gain is

$$G_{pa} = G_{pa1}G_{pa2} = 246 \text{ V V}^{-1} , \qquad (5.30)$$

which satisfies the gain requirements determined in section a1. The voltage noise of PA2 is 12 nV/√Hz, and when combined with the thermal noise of resistances 17 and 18, which are 2k4 Ω and 12 kΩ respectively, gives a voltage noise of 13 nV/√Hz. Even if the total voltage noise of the remaining video processing circuitry has the unreasonably high value of 90 nV/√Hz at the output of PA2, the total input noise to PA2, excluding that of PA1, is only 20 nV/√Hz. As has been shown, this value does not contribute to the net noise of the video processing electronics because of the value of G_{pa1}.

The power supply filter for the PA1 amplifiers use a 47 μF capacitor in the negative power supply filter. This is because the output voltage is always negative, and so the dynamic current from the feedback network exits the amplifier through the negative power supply pin. The larger capacitor ensures that the amplitude of the ripple voltage, due to the power suuply filter resistor in the power supply line, is sufficently small that it can be completely rejected by the power supply rejection ratio of the amplifier.

The final parameter of the preamplifier is the net video leakage current from PA1 and the reset switch. Measurements of that current indicate that when the dewar and preamplifier are at equilibrium temperatures, its value is

$$i_v = 1 \text{ pA} . \qquad (5.31)$$

The video voltage changes at a constant rate due to the accumulation of leakage current charge on the video capacitance. During the 250 μs interval in which the leakage current is contributing to the output signal, determined in section 5.4.3, an equivalent signal of 1600 e^-/h pairs is accumulated. It follows that this signal is fully tractible as a component of the fixed pattern if the video current varies by no more than ≈10%, and that baseline instability results if the variation is larger than this. Variations result from dependences upon the ambient temperature of the

devices, and upon the video voltage. Inspection of the OPA102BM curves of leakage current versus these parameters indicates that the requirements are satisfied if the ambient temperature remains constant to within several degrees between the image and fixed-pattern readouts.

d) Hardware Implementation

The four preamplifiers are implemented as shown in plate 5.1, with the printed circuit board shown in figure 5.4, and in appendix 11. The board is circular so as to fit within the cavity of the dewar that is seen in figure 4.1. Because there is no room for connectors on the board, a second board that can be seen in those illustrations is used for that purpose. The boards are mounted to each other with standard electronic 0.64 mm square pins which connect their respective ground planes together. Similar pins carry the signals between the Connhex 50Ω co-axial connectors on the bottom

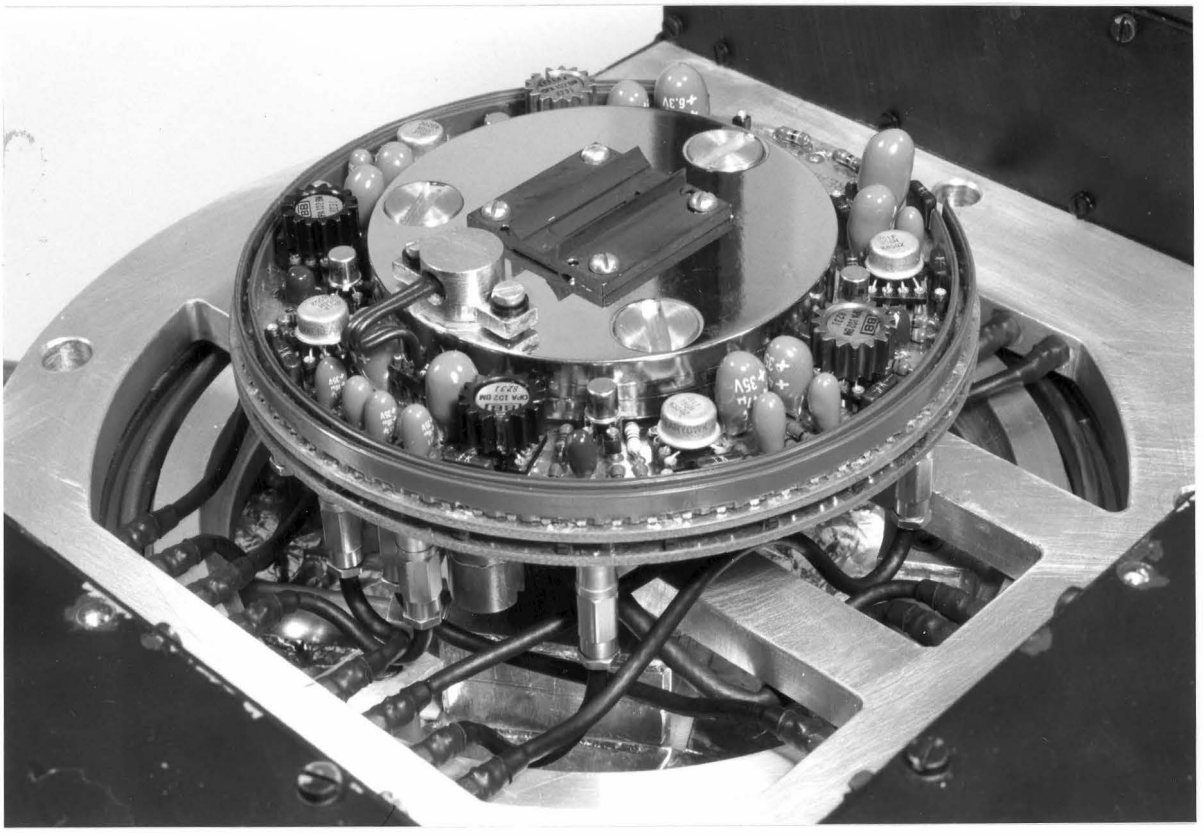


Plate 5.1: The LDA preamplifier board and cold block.

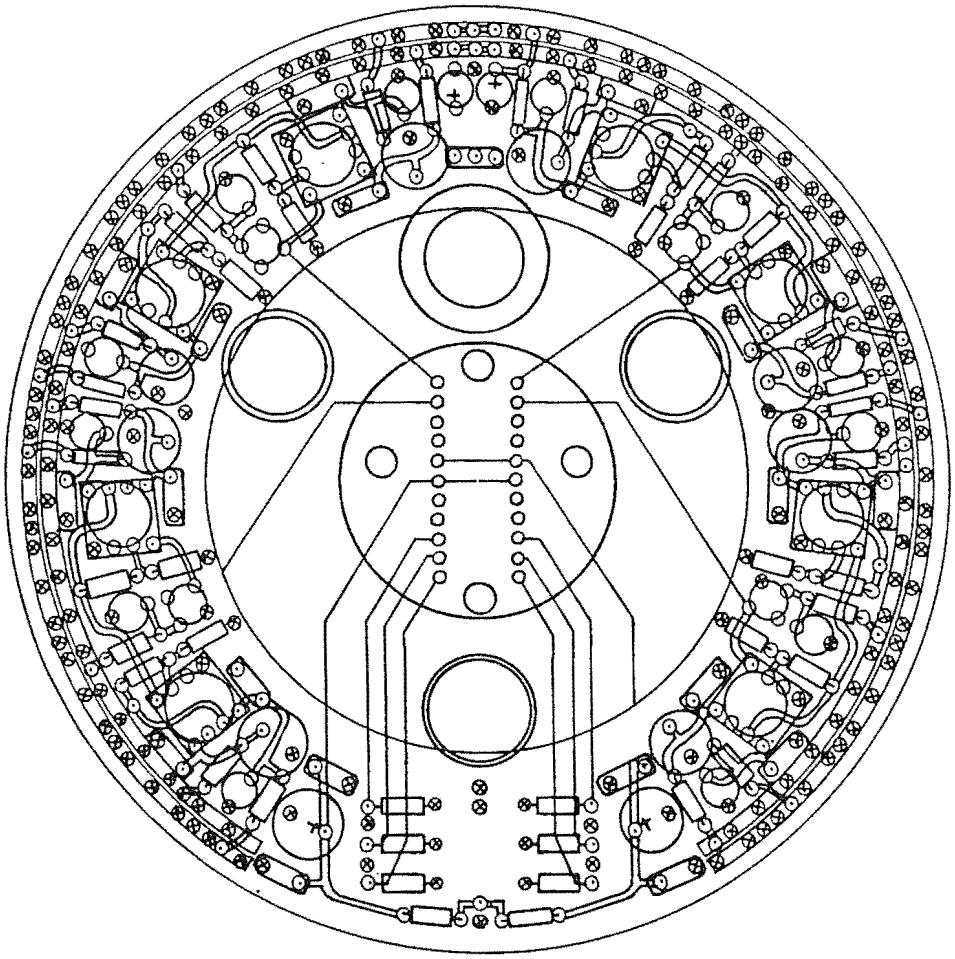


Figure 5.4: Printed circuit board layout for the preamplifier electronics given in figure 5.3.

board, and the circuitry on the top board. The top board is screwed to the pedestal on the cold block so as to locate the preamplifiers.

The conection between the preamplifier ground plane and the cold block ensures that the block acts as a shield around the array, and above the circuitry board. A solid ground plane over the entire top surface of the connector board acts as the electrostatic shield over the bottom side of the circuitry board, and in particular, shield the high impedance video lines, and the low signal level circuitry that is on the bottom side of that board.

The diode array is mounted on the two strip sockets shown in figure 5.5, which are soldered to the signal tracks on the circuitry board which connect the array to the external circuitry. Each track has a matching ground track on the opposite side of the board along its route to that circuitry

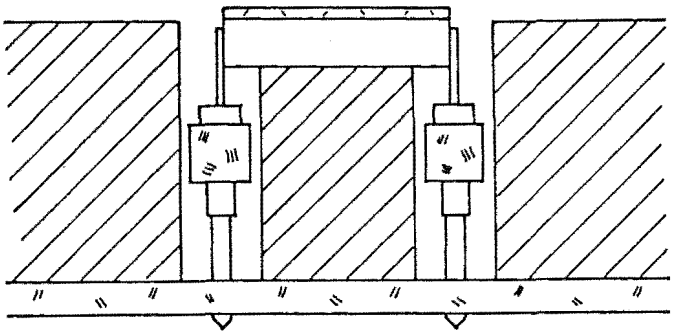


Figure 5.5: Cross-section of the cold block, showing the LDA mounted in its sockets.

so that the signal remains shielded and tightly coupled to ground.

The temperature at the centre of the circuitry board is that of the cold block, while the temperature of circuitry area is close to that of the flange because of the connection of the flange to the ground plane through the shielding on the co-axial cables. Therefore a temperature difference of approximately 130°C exists across the annular gap in the ground plane of that board. This gap prevents excessive thermal leakage through the thermally conductive ground plane, which would rapidly expend the cryogen. For this same reason, the cross-sectional area of the signal lines is minimized by their having the smallest practical size of 0.4 mm. The net leakage through the conductive tracks and the circuit board can be calculated to be ≈1.6 watts.

The high impedance video line areas of the printed circuit board and components are treated to prevent surface leakage currents from being a significant component of the video leakage current. The treatment is a light application with a mixture made from ≈10 ml of benzene and several drops of silicone oil. The benzene lifts the contaminants above the surface so that the silicone can form a uniform high impedance coating in their place. It is most important that the coating is not touched after it has been applied because contact breaks the coating so that finger oils can reach the surface.

5.3.3 Video Amplification

A final stage of amplification is needed to achieve the gain required by result 5.9.

a) Requirements

The full video processing gain was not applied with the preamplifiers because their pure non-inverting configuration would have resulted in the saturation of the output stage, as discussed in section 5.3.1. By using equation 5.11 and 5.28 with result 5.14, it follows that the output video signal is in the range of -12.3 volts to -8.0 volts. Therefore if that range is offset so as to be centred about 0 volts, additional gain can be applied.

As demonstrated in appendix 1 with figure A1.1 and equation A1.4, an inverting amplifier can be used to both amplify and offset the signal. The required gain of this video offsetting stage is found from equations 5.10 and 5.14 to be

$$|G_{vo,lo}| = \frac{G_{vp}}{G_{pa}} = 3.78 \text{ V V}^{-1} \quad . \tag{5.32}$$

After this amplification, the amplitude of a full scale signal will be the required $\Delta V_{A/D,fs}$= 10 volts. For this range to be centred on 0 volts, and taking into account the negative sign of the G_{vo}, the input voltage of -12.3 volts must become an output voltage of +5 volts. Given these two voltages and result 5.32, equation A1.4 can be solved for the voltage that is necessary at the non-inverting terminal in order to produce the required offset. It is found to be

$$V_{i+,lo} \approx -8.7 \text{ volts} \quad . \tag{5.33}$$

The maximum signal size was found to be 2.73 M e^-/h pairs in result 5.11. This may be inadequate for extremely high signal-to-noise ratio work, and so a second set of options will be made available to extend that range by a factor of 2.5 to

$$q_{A/D,fs,hi} = 6.8 \text{ M}e^-\text{/h pairs} \quad . \tag{5.34}$$

It follows that the gain of the video offsetting stage must be

$$G_{vo,hi} = 1.51 \text{ V V}^{-1} , \quad (5.35)$$

that the voltage at the non-inverting input must be

$$V_{i+,hi} = -5.5 \text{ volts} , \quad (5.36)$$

and that the signal equivalent of the LSB of the A/D convertor is

$$q_{A/D,hi} = 418 \text{ e}^{-}/\text{h pairs} . \quad (5.37)$$

b) Circuitry

The negative video offset voltages are generated from the video offset reference, VOR, shown in figure 5.6. The

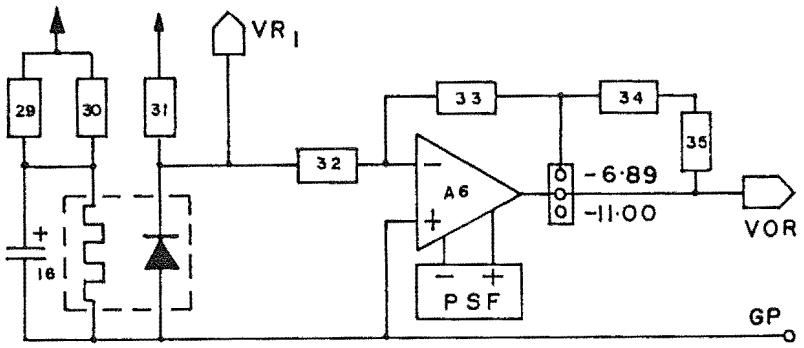


Figure 5.6: Video offset reference (VOR) voltage circuit.

LM399 precision voltage reference that is used to generate the diode array bias supply, is inverted by amplifier A6. The mini-jump can be used to change the value of the feedback resistance so that VOR has two possible values. The resistors are set so that the quotient of those two values is equal to the quotient of the non-nonverting input voltages in results 5.33 and 5.36. This will allow a single resistor divider network to produce either of the offset voltages by simply changing the position of the mini-jump.

Resistors 32 and 33 are of the precision type discussed in section 3.2.4c, which enable the total temperature coefficient of VOR to be kept below ≈4 ppm $(C^{o})^{-1}$. Its voltage spectral noise density is approximately 18 nV/√Hz.

The amplifier which performs these two tasks is the first stage of the video processing electronics which are shown in figure 5.7. The preamplified video signal number n, PV_n, is shown driving the amplifier, and can be amplified by

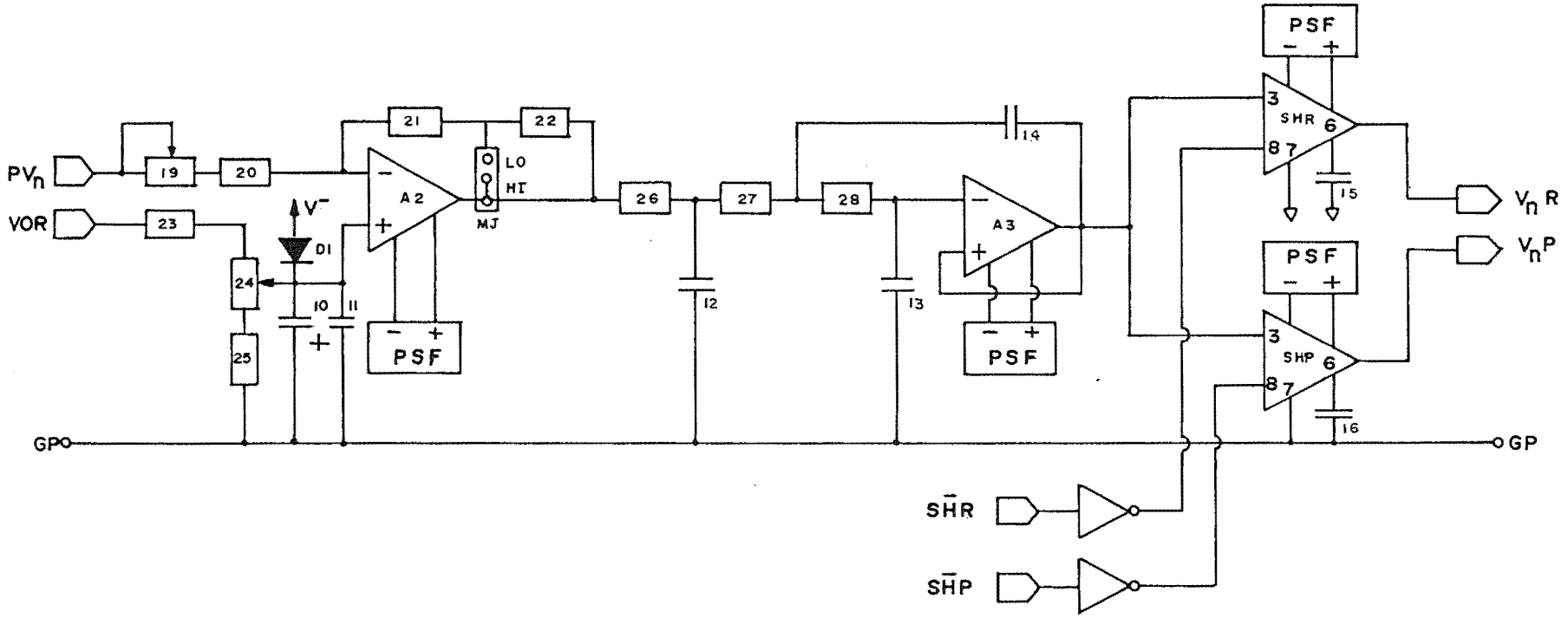


Figure 5.7: Video processing electronic circuit.

one of the two required gains which are selected with the mini-jump. Variable resistor 19 allows the gain of each video line to be individually adjusted so that the net gain of all four lines is the same. The signal is offset as a result of the network of resistances 23, 24, and 25 dividing VOR down to the required value, and variable resistor 24 is used to make small adjustments for the characteristics of the particular video line being offset. The value of VOR must be correctly selected for the gain value being used, because only two of the four possible combinations of the mini-jump positions are valid. Capacitors 9 and 10 combine with the output resistance of the divider network to filter VOR with a pole frequency of ≈10 Hz, and diode 1 protects the amplifier input terminal from the energy of the capacitor as it discharges during power-down.

c) Hardware Implementation

The video processing circuitry is implemented on the printed circuit board shown in plate 5.2, which has the layout

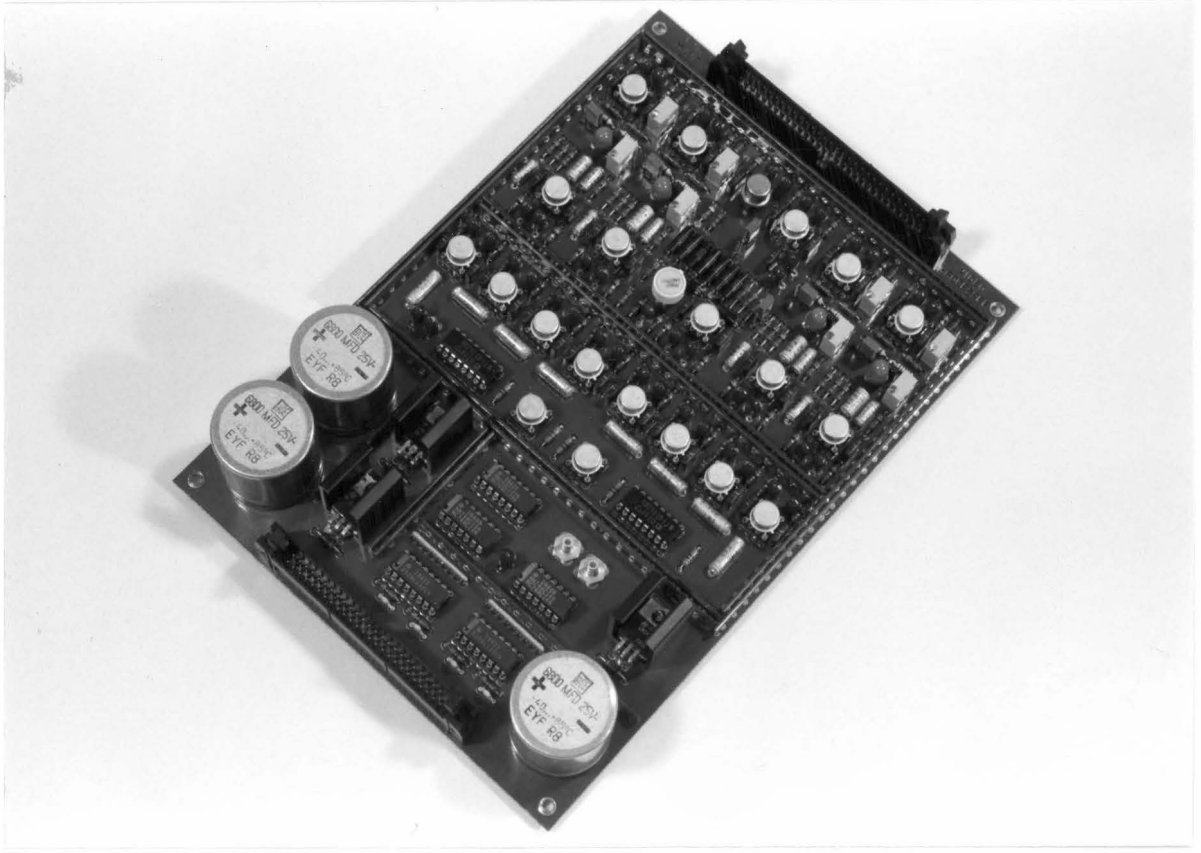


Plate 5.2: The video processing printed circuit board.

that is shown in figure 5.8. Two of the four video offsetting and final amplification stages are on either side of the bias supply across the top of the board. The variable resistors above the amplifiers are for the fine adjustments of the individual gains, and the variable resistors below the amplifiers are for the fine adjustments of the individual offsets.

The video offset reference and the precision reference are located below the bias supply, and the offset-selecting mini-jump is above them to the right.

5.4 Video Signal Extraction and Noise Rejection

The video signal has been amplified to the required level with a design that exhibits a low intrinsic noise, and which generates a minimum of excess noise due to instability. The data encoded in that signal must now be extracted, and the components of its noise from the electronic design and the diode array must be reduced so as to meet their design requirements.

5.4.1 Correlated Double Sampling

The data in the video signal from a detector using the voltage level readout technique can be determined by a signal extraction and processing technique that has been developed by White et al. (1974), which they have called correlated double sampling. In addition to signal extraction, the action of correlated double sampling is a technique for rejecting video noise.

a) Signal Extraction

The datum in the video signal of a given diode (described in section 2.2.1b) is the difference between the video levels before and after the diode is read out. These video levels are shown in figure 2.7, and are respectively called the reset and signal levels. Correlated double sampling extracts this datum by sampling and holding each of those levels, and then taking their difference to form the

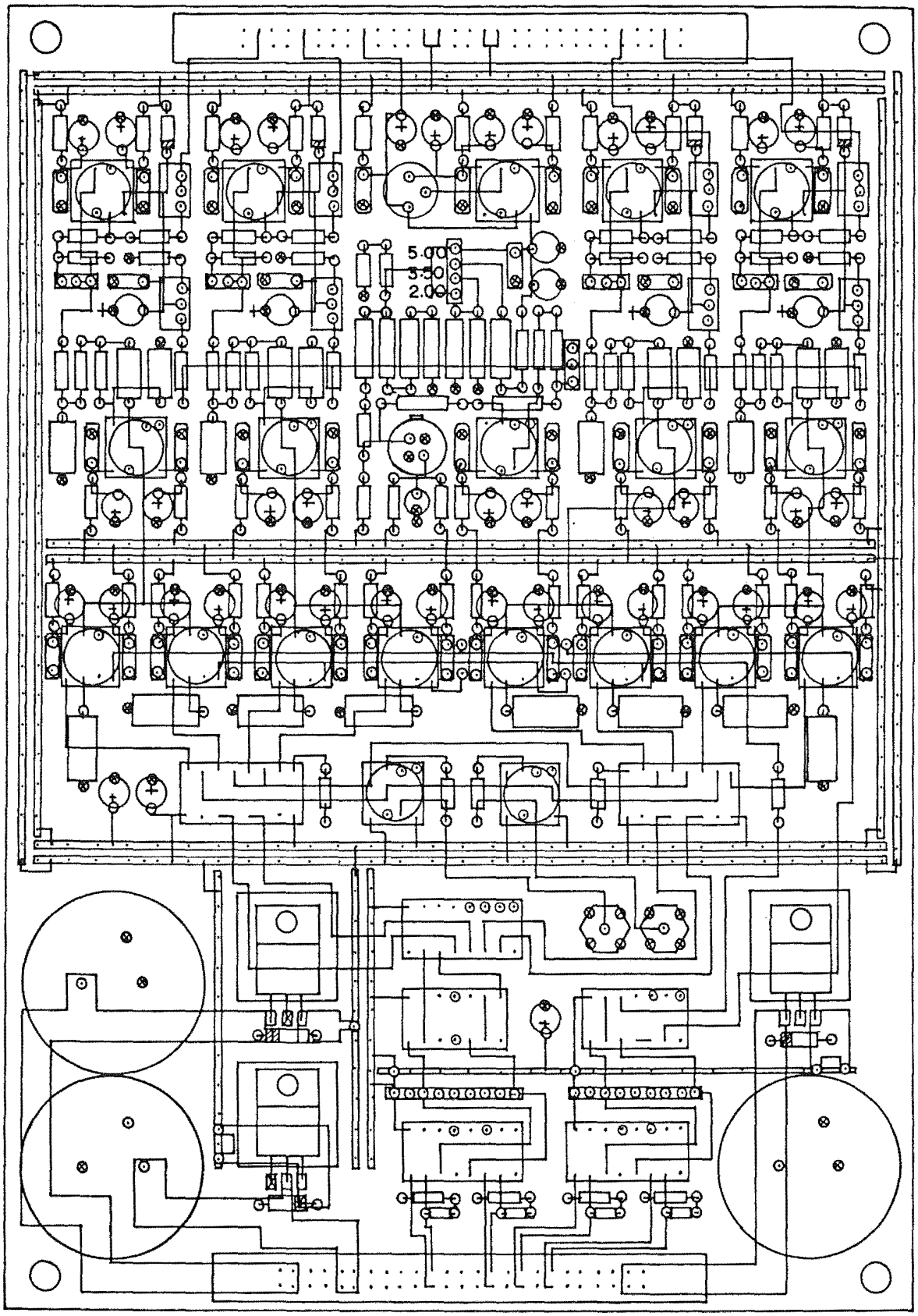


Figure 5.8: Printed circuit board layout for video processing electronics.

signal that is quantified by equation 2.8. It follows that there are three essential components of correlated double sampling. Two of them are sample and hold components, with one being used for each of the reset and pixel levels, and the third is a differencer which forms the difference of the held outputs of the sample and hold components.

b) Thermodynamic Noise Rejection

Unlike most noise sources, the thermodynamic noise of the video and diode capacitances (described in section 2.1.6a) are simple offsets to the video voltage whose amplitudes are determined at the instant the reset switch opens. In the case of the video capacitance, that capacitance remains physically unchanged when the diode is read out, and so the readout process does not change its noise contribution on the video line. Therefore when the reset and pixel level samples are differenced by correlated double sampling, the noise of the video capacitance is completely rejected. This is essential because the thermodynamic noise of this capacitance, which can be found from equation 2.3 and result 5.7 to be 1750 e^-/h pairs, is considerably higher than the system readout noise requirement.

The second case is that of the diode capacitance. When diode n is being processed, the reset level that is held by the correlated double sampler is that of diode n-1. Therefore when diode n is switched onto the video line, the thermodynaic noise charge from diode n-1 is left on the video line, and the thermodynamic noise from the previous initialization of diode n is added to the video line. Thus the diode thermodynamic noise is uncorrelated between the samples of the reset and pixel levels, and therefore it cannot be removed by correlated double sampling.

c) Noise Filtering Response

While correlated double sampling can completely remove noise that is correlated between its two samples, its action can also attenuate noise that is uncorrelated between those

samples. Consider the worst-case example of a noise component of frequency f, and therefore period T, which is sampled symmetrically about its zero crossing. If the time between samples is T_s, corresponding to a sampling frequency of f_s, the fraction of the noise amplitude that appears at the output of the correlated double sampler is

$$A_{cds} = \frac{\sin\left[\frac{2\pi}{T}\left[\frac{T_s}{2}\right]\right] - \sin\left[\frac{2\pi}{T}\left[-\frac{T_s}{2}\right]\right]}{(1 - (-1))} . \qquad (5.38)$$

When rearranged and expressed in terms of the frequencies, this expression becomes

$$A_{cds}(f_s, f) = \sin\left[\pi \frac{f}{f_s}\right] . \qquad (5.39)$$

The quantity A_{cds} can be interpreted as the minimum attenuation that a correlated double sampler operating at a frequency f_s can apply to a noise component of frequency f. It shows that low frequency noise is strongly attenuated, and that the dc component is completely removed. This bandwidth limiting action is one such action used in the video processing electronics, and shall be combined with the other responses in section 5.4.3.

5.4.2 Bandwidth Limiting

The reset and pixel levels are instantaneously sampled by the correlated double sampler. Therefore random noise on the video waveform will also be included in those samples, and so that noise must be minimized. This is achieved by forming an upper limit on the video bandwidth that is equal to the lowest value which will still allow the video information to pass to the correlated double sampler.

a) Resetable Integrator

Livingston et al. (1976) state that for white noise (see appendix 2), the use of an integrator gives the lowest noise bandwidth. Indeed most diode array systems use an integrator to bandwidth limit the video noise by individually integrating the reset and pixel level signals. Because the

input signal is a level, the output signal is a linear ramp which must be sampled at the end of the integration time by the correlated double sampler. Consideration of the specification sheets for commercial sample and hold units shows that their dynamic sampling error is proportional to the rate of change of their input signal. If the input signal was purely the required diode datum, this linear source of error would be fully tractable by the flat-fielding process. In general, however, a large component of the input signal is due to offsets, and therefore variations in those offsets will appear as noise if the dynamic sampling error is large. This problem can be avoided with a bandwidth limiting filter which settles to a constant output level before the time at which the samples are taken.

b) Bessel 3-pole Low-pass Filter

For a step input, the Bessel-type of low-pass filter settles to any specified accuracy in the fastest time. It follows that it can have the lowest bandwidth of any filter used in this way. Therefore a 3-pole Bessel filter will be used to bandwidth limit the video signal before it is passed to the correlated double sampler. One advantage of this filter is that it settles to a constant level when it has acquired the input signal, and therefore dynamic sampling errors do not occur in the subsequent sampling. Other advantages include not requiring the reset switch and reset logic of the resetable integrator, and having a much higher attenuation at high frequencies.

The required pole frequency can be determined by modelling the response of this filter type to the video signal. The same procedure has been used as was described in section 4.2.2b for the temperature controller. One of the differences is that the transfer function of the filter is used instead of the temperature controller transfer function, and the other is that the input waveform is the video signal. A Fourier series of the video signal shown in figure 2.7 can be formed as the sum of the series for a square wave, and the series for a non-50% duty cycle waveform. This second series is used to represent the reset pulse feedthrough on the video signal. Different choices for the ratio of the amplitudes of

those waveforms allows different signal levels to be modelled. The curve shown in figure 5.9 is the response of the final design to the worst case input signal, which is the maximum negative signal step combined with the reset feedthrough pulse. It uses a 600 ns reset pulse width as determined in section 5.3.2c, and a pole frequency of 6.0 kHz (which corresponds to a time constant of 1.67 μs). It shows that a period of 1.5 time constants must elapse in order for the filter output voltage to settle to an acceptable accuracy of $\approx$0.7 mV (equivalent to $\approx$1 LSB). This length is equal to the 250 μs period that is available for the given video level to be interrogated.

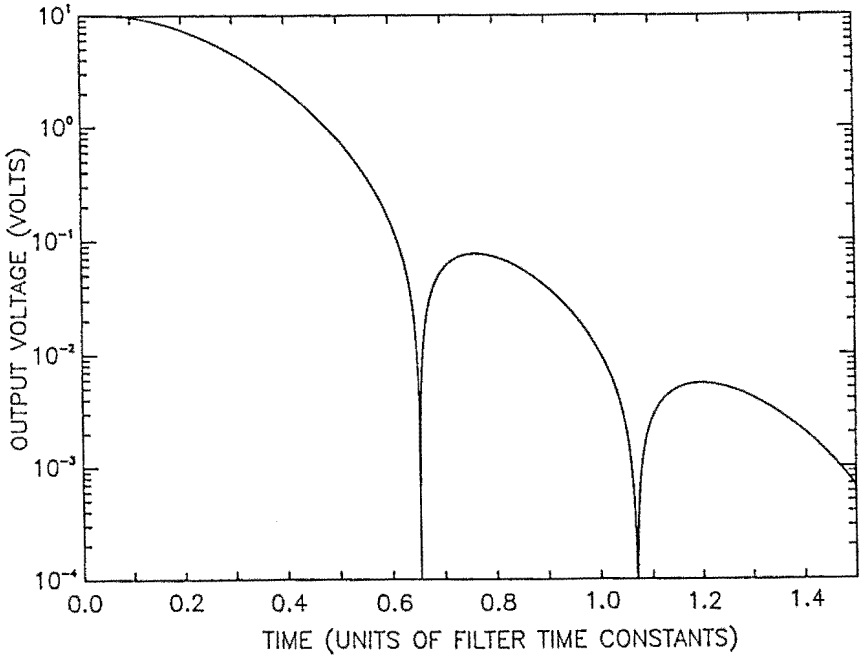


Figure 5.9: Response of the low-pass filter to the maximum video reset step.

5.4.3 Video Processing Transfer Function

The net transfer function of the video processing electronics is the product of the transfer function of the low-pass filter, and the response of the correlated double sampler that was given in equation 5.39. The time between samples follows from section 5.1.2 and figure 2.7, giving T_s = 250 μs. The transfer function is shown in figure 5.10 as the full curve, with the dashed envelope being the response of the low-pass filter by itself. The essential features of the video processing bandwidth limiting can be seen. The low

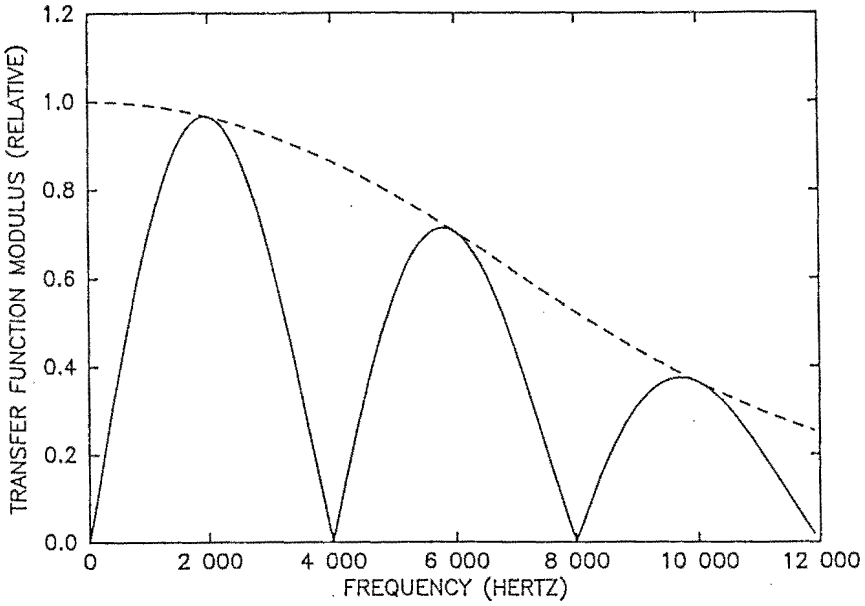


Figure 5.10: The transfer function of the video processing electronics (solid line), and the response of the low-pass filter (dashed line).

frequency attenuation is due to correlated double sampling, and the high frequency attenuation is due to the low-pass filter. However the attenuation is seen to be zero at the 2 kHz data frequency, and so while the noise is bandwidth limited, the data passes through unattenuated.

5.4.4 Reset Switch Action

The reset switch periodically connects the video line to ground. Any source of noise whose amplitude depends on how long the video line has been in a high impedance state will have a lower frequency limit (see appendix 3 for example) for its noise bandwidth which is set by the switching rate of that switch.

a) Video Current Noise Sources

In section 5.3.2a2, the contribution to the net voltage noise by the voltage equivalent of the video current noise was found to depend on the video line impedance. This equivalent noise voltage amplitude is due to the accumulation of charge on the video capacitance from the noise current. Therefore, the longer the video line is in a high impedance state, the

greater is the contribution from the low frequency components of the noise current.

The low frequency limit of the noise bandwidth for this source must therefore be the switching rate, f_s, of the reset switch. Consequently, the transfer function that the reset switch applies to the noise, due to this limit is

$$TF_{rs} = \frac{1}{\sqrt{1 + \left[\frac{f_s}{f}\right]^2}} \quad , \qquad (5.40)$$

which is the transfer function of a high-pass filter. Therefore, the equivalent voltage amplitude of the frequency components below f_s will be increasingly attenuated as the frequency decreases, until they are zero at dc. This transfer function combines with the video processing transfer function to bandwidth limit the video current noise. The net amplitude of the current noise which passes this bandwidth can be determined by including the square of the net transfer function in the integral given in equation 5.22. An approximate worst case evaluation of this integral has found that the net noise is significantly less than 100 e^-/h pairs. An exact evaluation will be performed using the REDUCE package at a later stage.

5.5 Video Processing Circuitry and Hardware

The circuit diagram for the video processing elctronics was given in figure 5.7, and the corresponding printed circuit board was shown in plate 5.2. The low-pass filter is formed with amplifier A3, resistors 26, 27, and 28, and capacitors 11, 12, and 13. The output signal from this filter goes to the two LF398 sample and hold devices, with the SHR device being used for the reset level, and the SHP device being used for the pixel level. The difference between their output levels is the data for the diode under interrogation.

The four low-pass filters, one for each video line, are located below their respective variable gain amplifiers on the printed circuit board. The eight sample and hold devices are in turn located under their respective low-pass filters. The four video lines are kept separate up until this point so that the video processing electronics for each line are given the

maximum possible time to reject the noise of the diodes that they process. However it is not necessary to have an A/D convertor for each video line, and so the four differential video lines are multiplexed into a single differential video signal with the circuitry shown in figure 5.11. The two switch banks, SW1 and SW2, are AD7511DI devices. The pairs of switches which correspond to the four video lines are selected by the address decoder, AD1, which is a high speed CMOS device providing the required logic levels for the switches. The output lines are buffered by the operational amplifers A4 and A5 which drive the signal to the A/D convertor electronics box. The switches are located on either side of these buffer amplifers immediately above the power supplies and line receivers on the video processing printed circuit board.

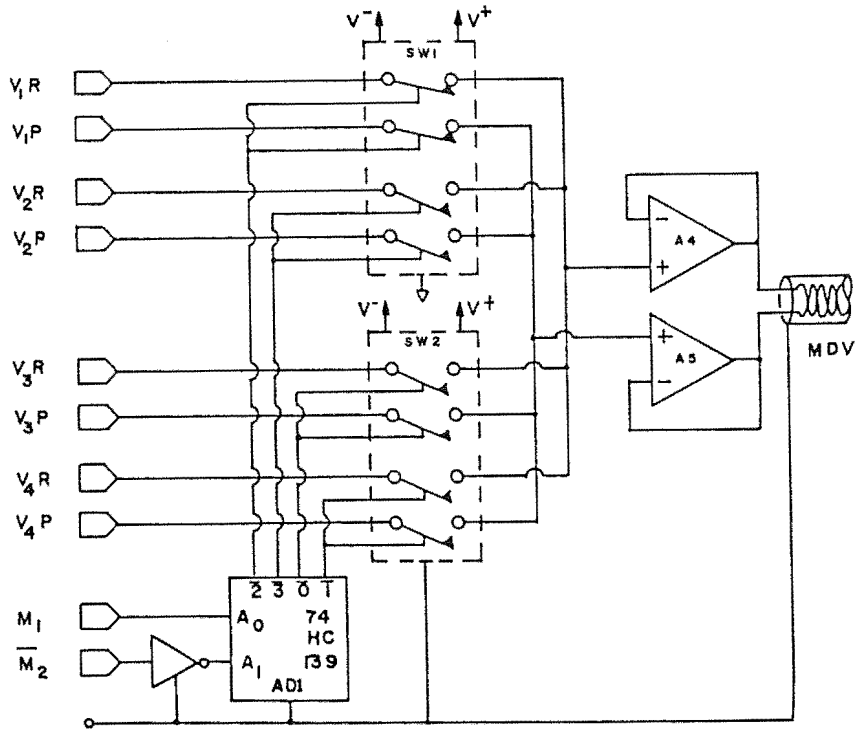


Figure 5.11: Electronic circuit showing the multiplexing of the four differential video lines (V_nR and V_nP).

An instrumentation amplifier was specified in section 3.2.3 for the interface between the video processing electronics and the A/D convertor electronics. Therefore the multiplexed video signal is transmitted to the A/D in differential form because that amplifier can perform the dual role of being the differencer for the correlated double sampling process.

The most important requirement on the differencer is that its common-mode rejection ratio is sufficiently high to reject the offset of the reset and pixel levels. In the worst case the offset would be 10 volts, and if it is required to be removed to an accuracy of better than 1 LSB, the common-mode rejection ratio must be greater than 90 dB (1 in 20,000). Consideration of the discussion given by Stout and Kaufman (1976, p.9-1 to 9-10) of the classical differencer, which is used by both Geary (1979) and Vogt (1982), indicates that it is extremely difficult to obtain the required performance from this design. Therefore the following alternative design has been implemented.

The differencer is the input stage of the A/D convertor circuit diagram that is given in figure 5.13. It is formed with two LF351 buffers, A12 and A13, and the Burr-Brown 3627 differential amplifier, DA. The common-mode rejection ratio has been measured as a function of frequency for this configuration, and the resulting data is given in figure 5.12. The data was reduced from the ratio of the input to output signal amplitudes when the inputs were joined together and driven with a sine wave generator. It is seen that the CMRR is 92 dB (1 in 40,000) at the 8 kHz data rate of the multiplexed differential video signal, and therefore the required performance is achieved. The output from the differencer is the multiplexed data from the array.

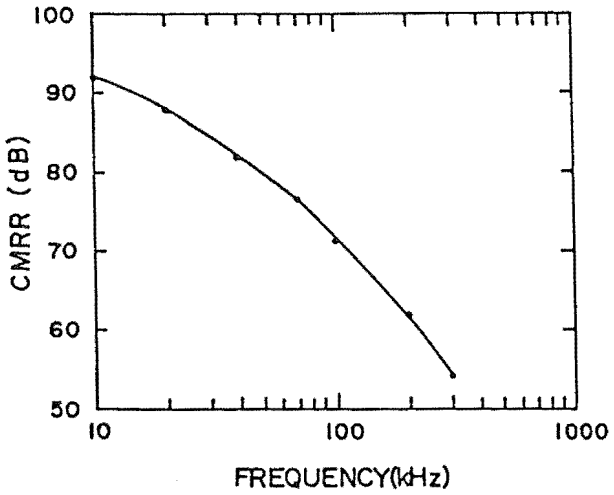


Figure 5.12: Difference amplifier common-mode rejection ratio (CMRR) as a function of the data rate frequency.

5.6 Analogue-to-digital Conversion

The conditioned multiplexed differential video signal must be received from the video processing electronics and digitized so that it is in a form that can be recorded by the Data Acquisition System, as will be discussed in Chapter 7.

5.6.1 Requirements

In keeping with the electronic functions in this work, the analogue-to-digital (A/D) conversion process is required to be performed by a commercial component. Such components can typically accept a range, called the full scale range, of analogue input signal which can be expressed as

$$\Delta V_{A/D,fs} = 10 \text{ volts} \quad , \tag{5.41}$$

and which will be assumed for this system. They resolve this range into 2 divisions of equal width, where n is usually 8, 10, 12, 14, or 16, which are sequentially labelled with an n-bit binary number. The digital output for a given input signal is the n-bit number of the division in which that signal falls, and is represented as an n-bit logic word. The width of a division is referred to as a least significant bit, and is given by

$$\Delta V_{LSB} = \frac{\Delta V_{A/D,fs}}{2^n} \text{ volts.} \tag{5.42}$$

To ensure maximum sensitivity from the detector system, the readout noise is required to be resolved by the A/D, that is, $\Delta V_{A/D,\sigma}$ must be approximately equal to 1 LSB. In real A/D convertors, the LSB width varies from division to division by an amount which is quantified by the differential non-linearity error of the convertor. This uncertainty in the digitization process is equivalent to a noise source, and so $\Delta V_{A/D,\sigma}$ must be sufficiently larger than the uncertainty to ensure that the contribution to the net noise is negligible. Therefore it will be made a requirement that the variation in the LSB width is less than approximately ±10% of $\Delta V_{A/D,\sigma}$. Manufacturer specification sheets and application guides show that typical good quality convertors, which are specified as

having no missing codes and a maximum differential non-linearity errors of ±½ LSB, have code widths within the range of 0.6 and 1.4 LSB. Therefore the requirement on this variation can be quantified as

$$\Delta V_{A/D,\sigma} \equiv 3 \text{ LSB} . \tag{5.43}$$

The number of bits that the digital word is required to have is a function of the required dynamic range of the detector. Using the definition of dynamic range in equation 1.10, it follows that the number of bits can be found from the expression

$$2^n \approx \left[\frac{q_{fs} - q_{fp}}{\sigma_r}\right] \Delta V_{A/D,\sigma} \text{ LSB} . \tag{5.44}$$

Therefore, substituting results 5.11, 2.1, 5.43, and requirement 5.1 gives the word size as

$$n = 14 . \tag{5.45}$$

The required linearity of the A/D conversion process can be determined using the system linearity requirement in section 5.1.1 with result 5.43. The result is that the peak non-linearity error must be less than ±1.5 LSB if their is no contribution to the non-linearity from the other video processing electronics. It follows that the maximum non-linearity of a typical A/D convertor, ±½ LSB, will provide an acceptable performance.

5.6.2 Electronic Circuits and Operation

The circuitry for the A/D convertor, its signal acquisition, and its data serialization are shown in figure 5.13. The data acquisition starts at the AD7511DI switch bank, SW2, which is used to direct one of the four possible signal sources to the A/D. The signals of those sources are the multiplexed video, the temperature controller heater power, and the block and ambient thermometers. The signal source is selected by the 74HC139 address decoder, AD_1, in response to the address lines A0 and A1. The decoder is high speed CMOS, because SW2 requires true 0 and 5 volt logic levels to achieve maximum performance.

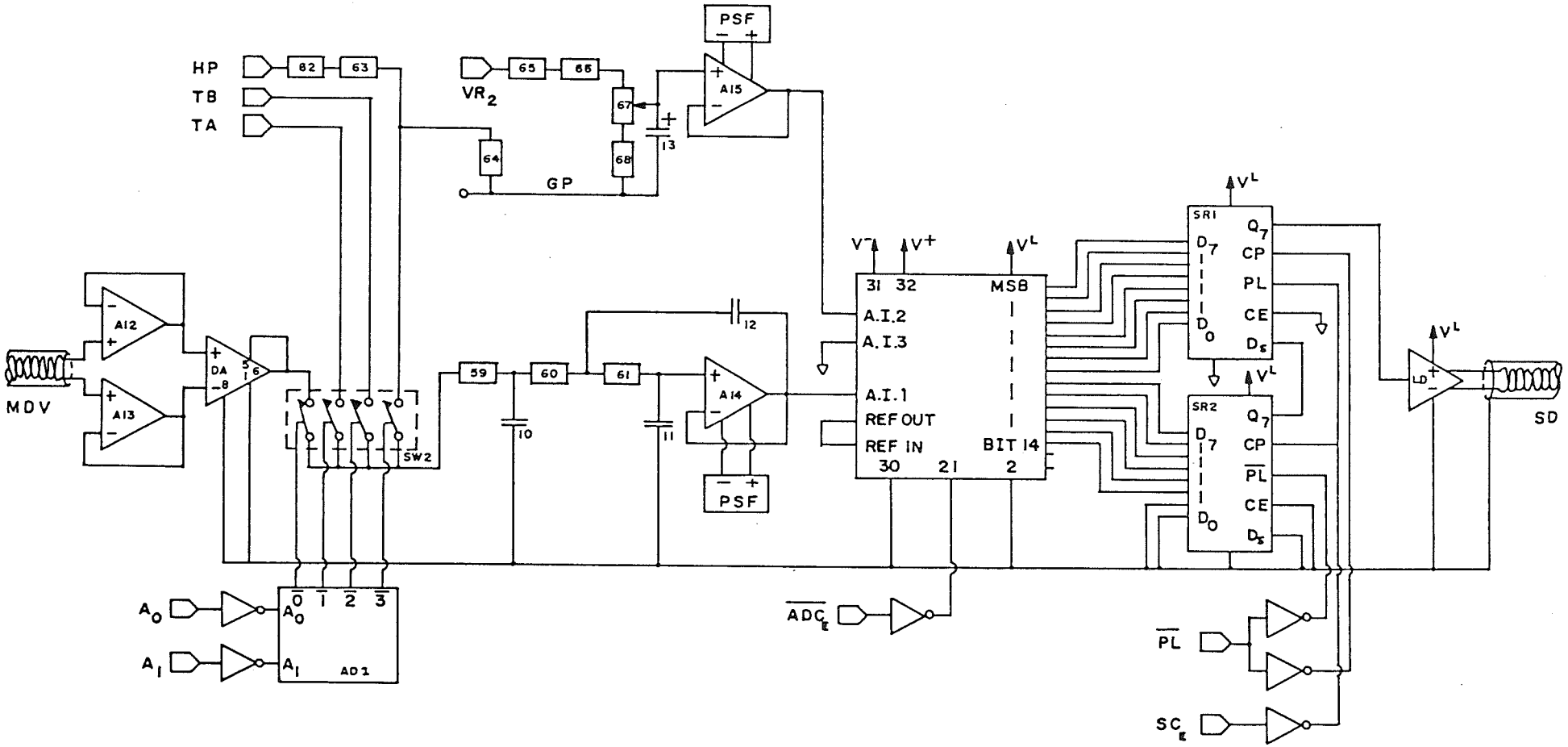


Figure 5.13: Electronic circuit for the A/D convertor, including its signal acquisition and data serialization.

The selected signal source is filtered by the 3-pole Bessel low-pass filter formed with amplifier A14. This ensures that the peak-to-peak level of the noise on the input signal is significantly less than 1 LSB. The pole frequency of the filter is 25 kHz, which requires a period of 55 μs for the step change in the input signal to be acquired to an accuracy of 1 part in 20,000. When convolved with the 35 μs response of the instrumentation amplifier, it follows that the start of the conversion for the video signal must occur approximately 90 μs after that source is selected. At the 8 kHz rate at which pixels must be converted, corresponding to 125 μs per pixel, the remaining 35 μs are available for performing the conversion.

The analogue-to-digital convertor is an Analog Devices ADC1140 16-bit convertor, whose 35 μs conversion time satisfies the above requirement. The performance for this convertor corresponds to a 14-bit convertor which has ½LSB linearity and differential non-linearity, and so the 15th and 16th bits are not used. It is less expensive and physically smaller than 14-bit devices which usually are designed to have very fast conversion times.

Because the fixed-pattern for a given video signal has positive and negative components for alternating diodes, the A/D input voltage range must be offset from the usual 0 to 10 volt input range so as to accommodate the negative components. This is achieved with the variable reference voltage that is supplied by amplifer A15 to the analogue input number 2, AI2, of the A/D convertor. A lower input range limit of $-V_1$ is achieved when the reference voltage is $+2V_1$.

The 14 output data lines of the convertor are received by the two 8-bit shift registers, SR1 and SR2. In response to the control signals described in the next section, the 14-bit parallel input data is output in serial from pin Q7 of SR1. These data are driven by the line driver, LD, to the interface chassis, which in turn drives it to an optocoupler in the Data Acuisition System as described in section 7.1.3b.

5.6.3 Conversion Timing

The timing waveforms for the analogue-to-digital conversion process and data serialization are shown in figure 5.14. The 1 μs width $\overline{ADC_e}$ pulse causes the start of conversion with its negative going edge. When the conversion has finished 35 μs later, the parallel data is loaded into the shift registers by the 1 μs low pulse of the $\overline{PL}$ control line, and the data available, $\overline{DAV}$, signal goes high to indicate that the data are not yet available. Fourteen pulses of 1 μs width are then issued on the serial clock line, $\overline{SC_e}$, whose successive positive going edges shift the parallel data by 1 bit through the shift registers. The bit which is shifted out of SR2 through pin Q7 is received by the input serial data line, D_s, of SR1. The stream of 14 bits which is shifted out through Q7 of SR1 is the serial data, SD, which are led by the most significant bit, and trailed by the least significant bit.

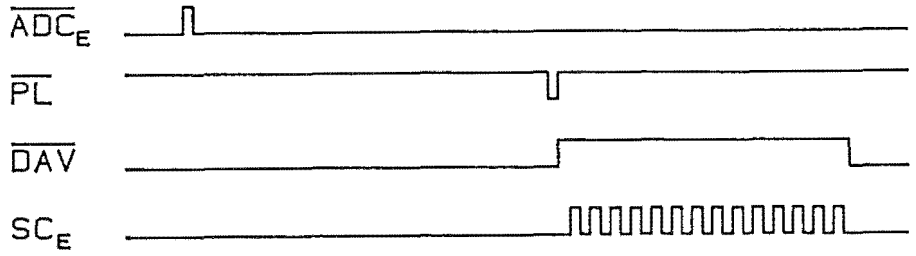


Figure 5.14: Control waveforms for the A/D and data serialization processes.

The serial clock is also used in the Data Acquisition System to clock the serial data into the serial-to-parallel shift registers. The incoming bits are clocked into those registers by the falling edge of the clock, which allows 1 μs for the data to propagate from the parallel-to-serial shift registers to the serial-to-parallel shift registers via the transmission line and interface chassis.

5.6.4 Hardware Implementation

The analogue-to-digital conversion circuitry, and the temperature controller and thermometer circuitry are implemented on the printed circuit board which is shown in

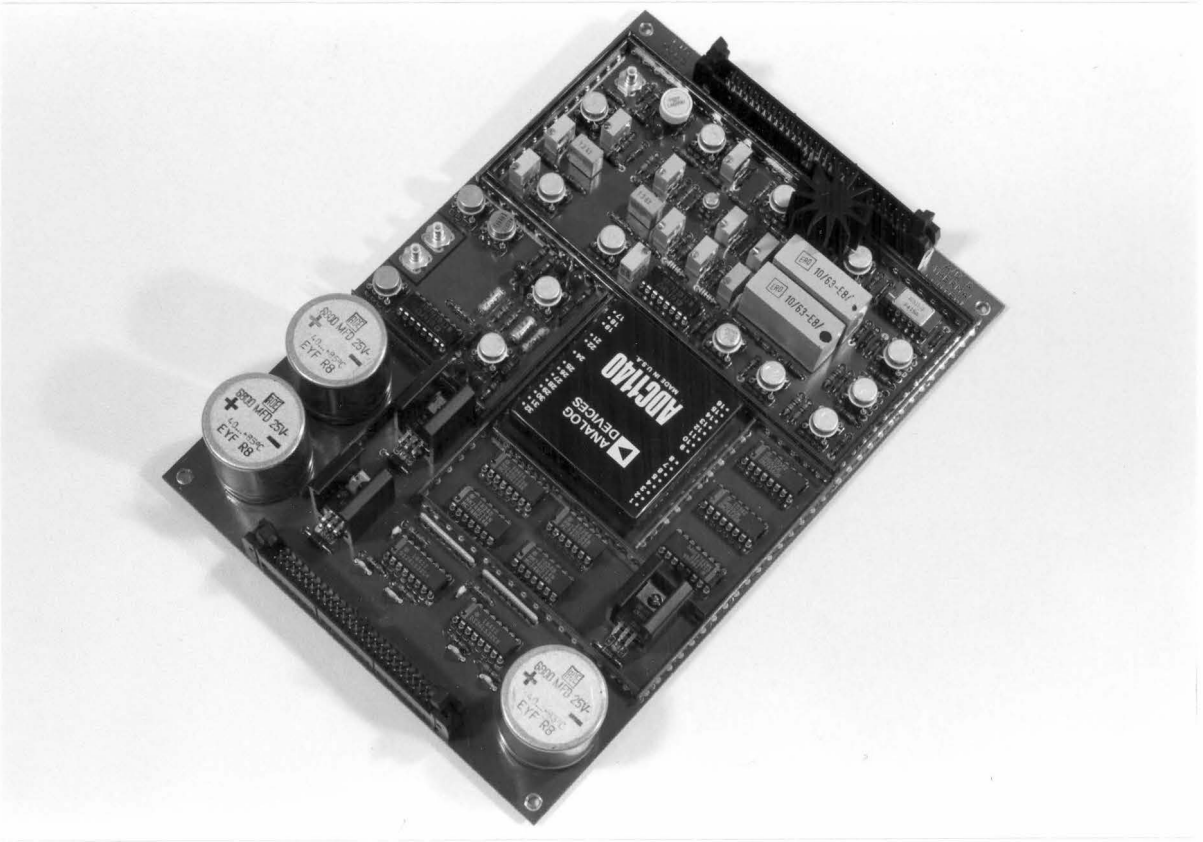


Plate 5.3: The A/D conversion and temperature controlling printed circuit board.

plate 5.3, and whose layout is given in figure 5.15. The bottom third of this board contains the power supplies, line receivers, and additional logic conditioning electronics. The A/D convertor is the module located in the centre of the board, and the shift registers for its data serializer are the top two chips on its right hand side. The differential line driver is located below them. The connectors on the far left of the A/D convertor receive the multiplexed differential analogue data from the video processing electronics. The shields of the connectors are isolated from the ground plane as was required for instrumentation amplifers in section 3.1.2b. The signals from these connectors are received by the buffer stages of the instrumentation amplifier, which are located above and below the connectors. Those signals are differenced by the 3627 differential amplifier, which is located to the right of the top input buffer, and the output signal goes to the A/D input source multiplex switch which is

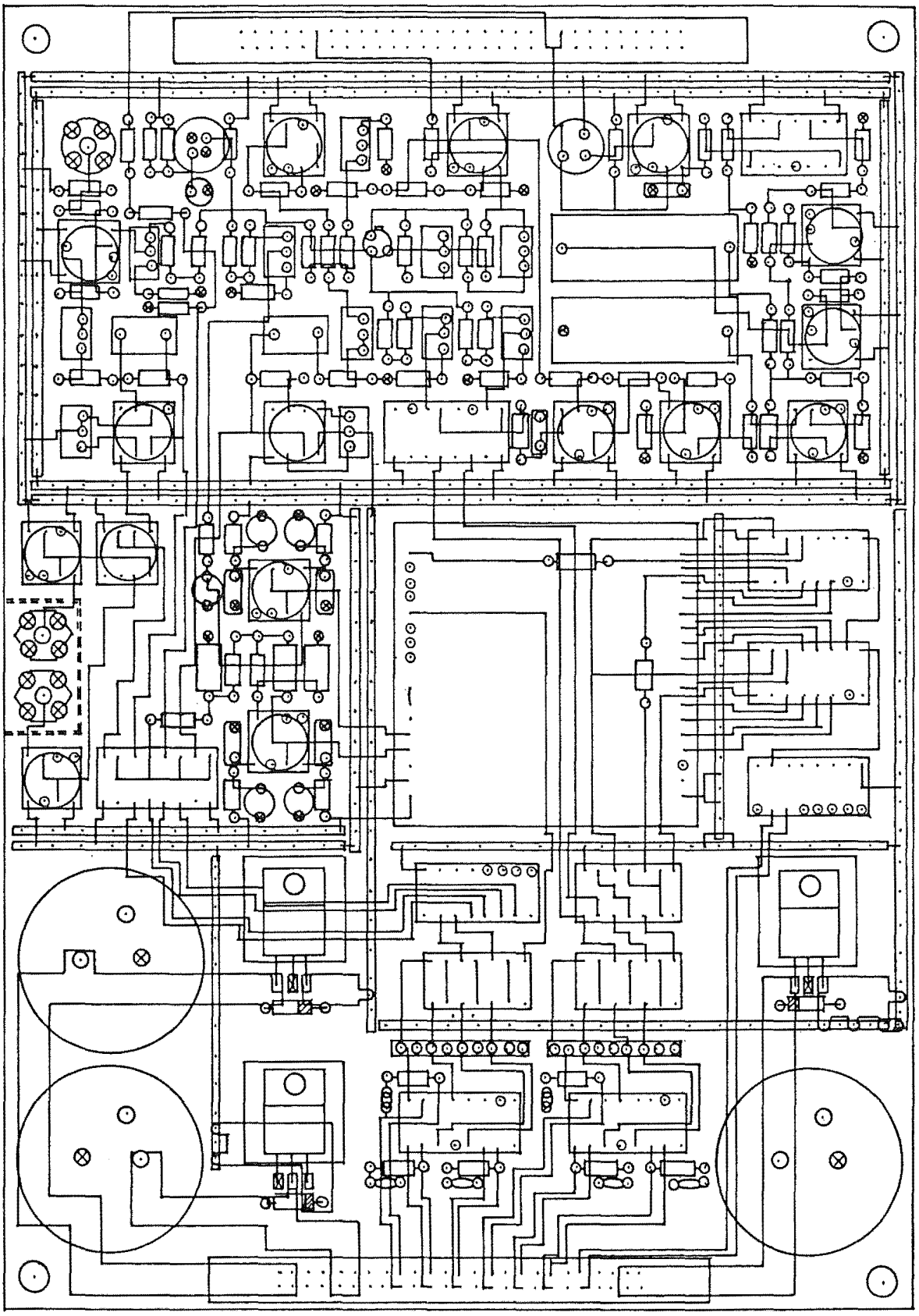


Figure 5.15: Printed circuit board layout for A/D conversion and temperature controlling electronics.

located to the right of the lower input buffer. The output from the switch goes to the A/D input filter located between the switch and convertor, and the A/D input offset amplifier is located above the filter.

The noise performance of the A/D convertor can be determined by connecting the input connectors to the ground plane, and then adjusting the A/D offset reference to determine what fraction of the LSB corresponds to the peak-to-peak input noise. The result is that the peak-to-peak noise is approximatley 30% of the LSB (bit 16), and so the A/D is essentially noiseless for the 14-bit precision being used.

5.7 Performance

The voltage noise source component of the video processing noise is the noise that is measured at the output of the video processing chain when the video lines are connected to ground. This is because the current noise sources are shorted to ground, and the concept of EMI coupling to the video lines becomes meaningless. However to perform this test, the video offset reference voltage must be zero volts because the video line is not offset by the reset logic feedthrough. The reference voltage can be set to zero by removing the LM399 reference, and connecting its former output pin to ground.

A typical noise gaussian that was measured in this configuration is given in figure 5.16a. It was formed from the difference of two readout frames, and is a plot of the frequency of occurrence of the possible difference values. The standard deviation of a single readout is $1/\sqrt{2}$ of the standard deviation of the fitted curve, which gives the noise as 200 e^-/h pairs. This value corresponds to a noise voltage amplitude of 0.8 μV on the video line, or a spectral noise voltage density of 9 $nV/\sqrt{Hz}$ within the noise bandwidth of the video processing electronics. This value is essentially equal to the theoretical 8.5 $nV/\sqrt{Hz}$ value that was given in result 5.29, and so, as required, the amplifier is the single dominant noise source in the video processing chain.

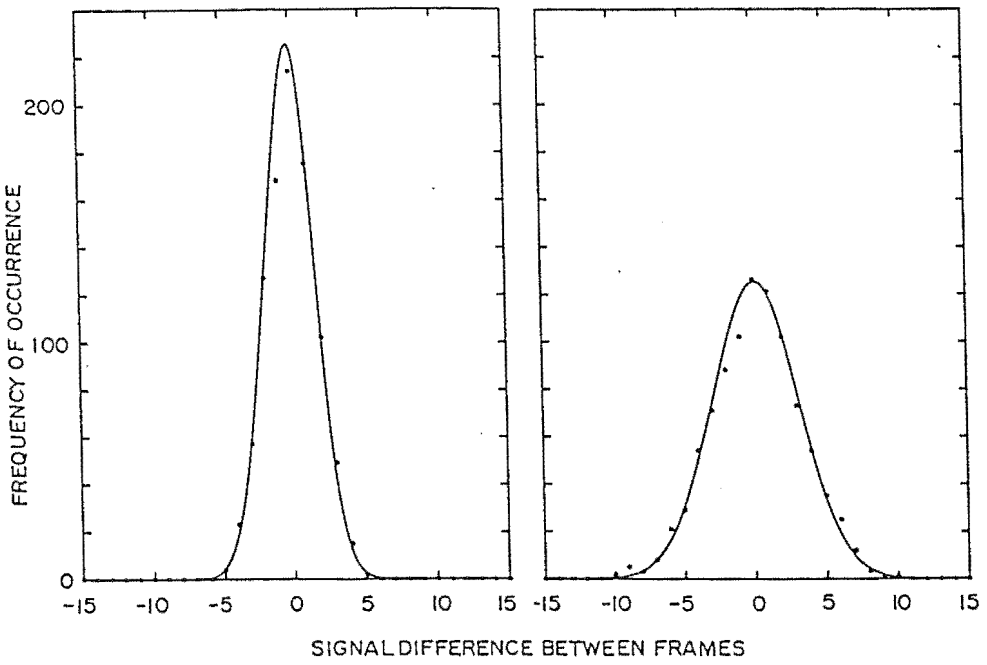


Figure 5.16: Noise Gaussian for the (a) low, and (b) high impedance cases of a noiseless signal source.

The readout noise that the system would exhibit if the diode array did not have thermodynamic noise can be determined by replacing the array with capacitors between the video lines and ground. The values of those capacitors are required to be equal to C_V. Using the same procedures as are outlined above, but with the normal video offset reference voltage, typical noise Gaussians like the one given in figure 5.16b are measured. The readout noise is 350 e^-/h pairs, which implies that an additional source of 290 e^-/h pairs exists due to current noise and EMI coupling when the video line is in the usual high impedance state.

Two readout noise Gaussians with the diode array installed are given in figures 5.17a,b. They are the only two that exist from the period before the array was damaged by electrostatic discharge. The readout noise from figure 5.17b is 450 e^-/h pairs, and the readout noise from the central 730 pixels in figure 5.17a is 400 e^-/h pairs. The extended wings correspond to the damaged pixels in the diode array. The difference between these values and the 350 e^-/h pair value found in the absence of the array can be entirely explained by the thermodynamic noise of the diode capacitances. It follows

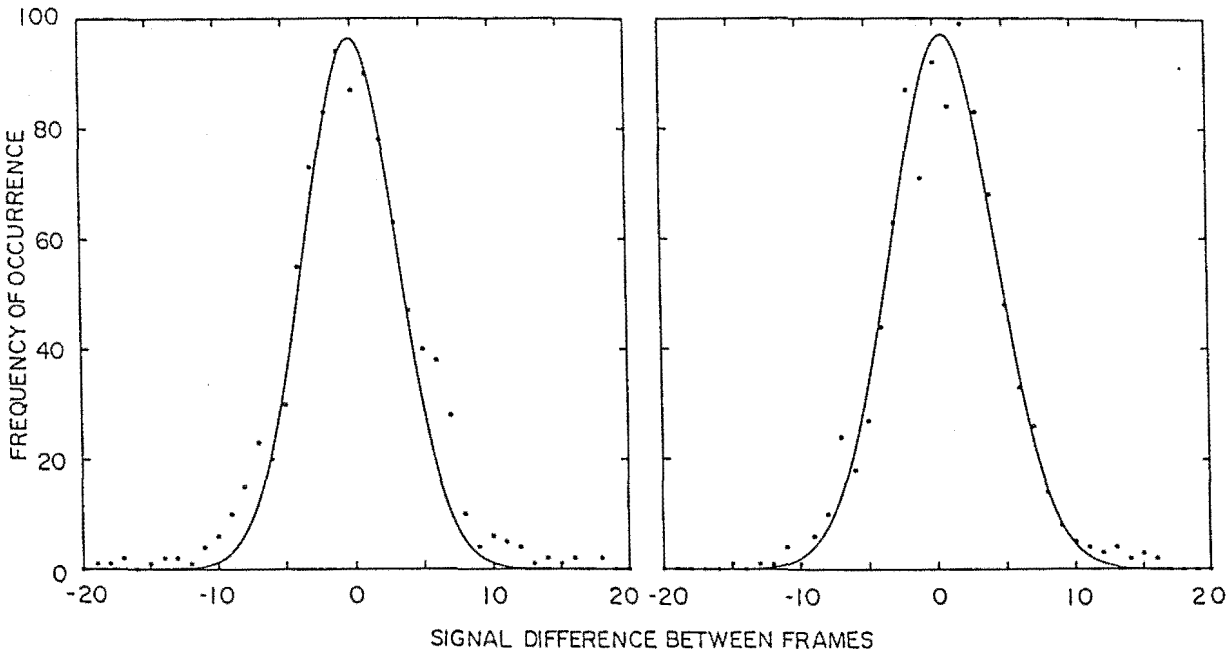


Figure 5.17: Noise Gaussians with the LDA under operating conditions.

that the readout noise from both the video processing electronics, and the entire system have met their design goals.

CHAPTER SIX

DIODE ARRAY CONTROLLING

The physical operation of the diode array and reset switches in response to their control signals has been given in sections 2.1.3 and 2.2.1 respectively. Some specific requirements for the characteristics of those control signals were deduced in section 2.4. In sections 3.2.1 and 3.2.2, the electromechanical design of the detector has taken into consideration the general requirements of the control signal generation, distribution, and conditioning. The generation of the control signals will be given in Chapter 7 , and their distribution has been given in section 3.3. It follows that the remaining requirements must be determined for the control signal conditioning electronics, and that their circuitry must be designed and explicitly fabricated.

6.1 Requirements

6.1.1 Reset Switch Control Logic

The amplitude, pulse width, and phase relative to the ϕ-clocks of the reset pulse have already been given in section 5.3.2c, and in section 2.2.1. The feedthrough of the reset signal, and therefore its noise, to the video line follows from section 5.3.2c as 1 part in 100 (-40 dB). If the amplitude of the noise from this source is required to be less than 1 nV/$\sqrt{\text{Hz}}$ on the video line, it follows that the noise of reset pulse logic levels is required to be less than 100 nV/$\sqrt{\text{Hz}}$.

6.1.2 Clocks and Start Pulse Logic

In addition to the requirements given in section 2.4, the Reticon RL series specification sheet given in appendix 6 either gives or implies the following additional requirements for the diode array control logic.

1) The clock amplitude must be approximately 12 volts, and the start pulse amplitude must be at least 10 volts,

2) the upper voltage level of the clocks and start pulse must be approximately equal to V_b, but not greater than V_b,

3) the logic level transitions should be as fast as is possible,

and 4) the clock electronics must be able to achieve this performance when driving the 50 pF input capacitance of the diode array clock lines.

An additional requirement follows from these as a consequence of the ability to change the bias voltage amplitude that was described in section 5.2.2. The upper and lower levels of the clock and start pulse logic must be able to be changed so that requirements 1 and 2 are satisfied for the three possible values of bias supply voltage.

A final requirement follows from the analysis of the response of the video-processing low-pass filter to the reset pulse. While the rising and falling edges of ϕ_1 and ϕ_2 are required in section 2.4 not to be cotemporal, they must be sufficiently close together that they appear to be cotemporal within the bandwidth of the video amplifiers. This will result in the input to the low-pass filter appearing as a single step input, rather than the underlying pair of complementary steps due to the complementary clocks coupling to the video line. The low-pass filter will therefore be able to settle in the minimum possible time.

6.2 Electronic circuits

6.2.1 Precision Power Supplies

The negative power supplies for the clock electronics, which determine the lower levels of the clocks, are generated from the precision voltage reference given in figure 6.1. This circuit, its operation, and its performance are essentially identical to the VOR reference described in section 5.3.3b. The 3.1 volt difference between the two possible output voltages corresponds to the 3 volt range of possible bias supply voltages.

The circuitry for one of those power supplies is given in figure 6.2. Its circuitry and operation are essentially the same as the bias supply described in section 5.2.2. The

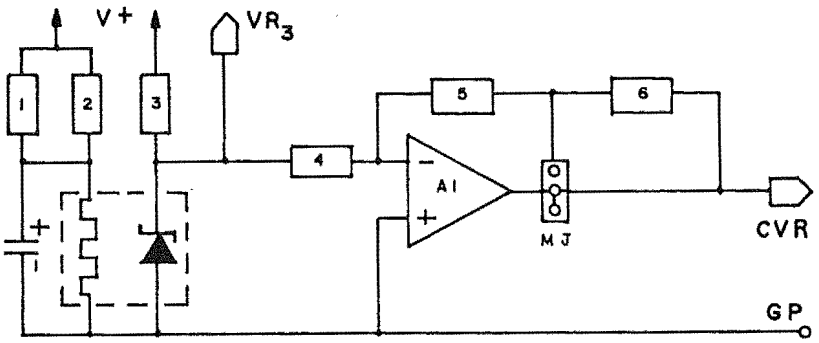


Figure 6.1: Electronic circuit for the precision voltage reference.

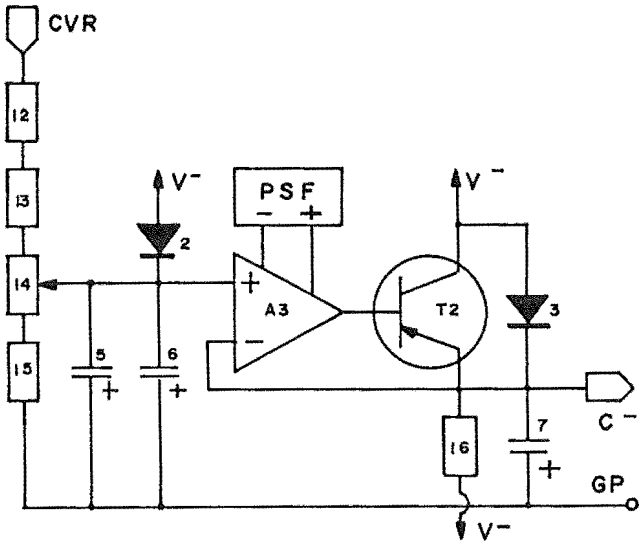


Figure 6.2: Electronic circuit for a negative power supply used by the clock electronics.

only significant differences are due to the opposite output polarity, which results in the polarized components being reversed, and the use of a PNP power transistor rather than an NPN transistor. Its noise performance is the same as that of the bias supply, but its temperature coefficient is slightly higher because because lower stabilty resistors are used in the resistor divider network. Diodes 2 and 3 protect their associated active devices from damage when the capacitances 5, 6, and 7 are discharged during power down.

The circuitry for one of the positive power supplies is given in figure 6.3, and its operation is also like that described for the bias supply in section 5.2.2. One of these power supplies is used with each pair of clocks for the two shift registers, and a third is used for the reset switch driver. In this third supply, the mini-jump and resistor 7

are omitted because step changes in the reset pulse amplitude are not required. The mini-jump selects either a 5.00 or 2.00 volt output voltage for the clock drivers, to correspond to the range of possible bias supply voltages.

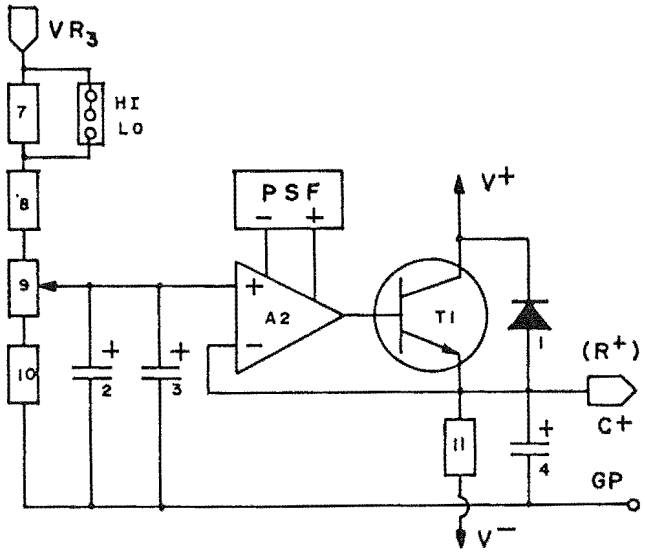


Figure 6.3: Electronic circuit for a positive power supply used by the clock electronics.

6.2.2 Reset Switch Drivers

Each pair of reset switches on the video line of a given shift register is driven with the circuitry given in figure 6.4. The high speed CMOS inverters (74HC04), I1 and

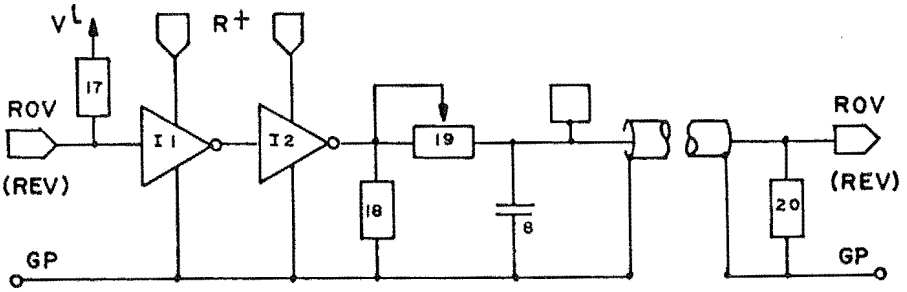


Figure 6.4: Electronic circuit used to drive reset switches.

I2, are powered by a precision reset switch power supply, R^+. They condition their input signal, ROV or REV, from the line receivers after that signal level has been pulled up by resistor 17 to meet the input level requirements of HC logic. Variable resistor 19 is used to bandwidth-limit the output level by its RC filter action with the optional capacitor 8, and with the capacitance of the signal distribution path. It

is set so that the rise and fall times of the reset pulse are just beginning to increase from their natural values. This ensures a minimum bandwidth for the noise on the reset levels, and therefore the minimum amount of noise feeding through onto the video line. Resistor 20 protects the reset switch from electrostatic discharge damage when it is disconnected from the protection of the reset driver logic. Like the optional resistor 18, it can be used as a pull-down resistor if its value is sufficiently low. This will ensure that the lower level of the reset logic is precisely the zero signal potential during the interval in which the diode is interogated. Changes in that level would feed through to the video line and thereby contribute to the fixed-pattern and readout noise.

6.2.3 The Start Pulse Logic

The start pulse control signal is conditioned with the circuitry shown in figure 6.5. The DS0026 MOS driver, I5, is used to condition this signal before it is applied to the diode array shift register. It translates the input signal from the line receiver to the C^+ and C^- levels required by that register in response to being driven by the ac coupled signal from the advanced low power Shotky drivers I3 and I4. Its output noise is bandwidth-limited, for the same reasons as were given for the reset logic, with variable resistor 21 and optional capacitor 10. The 510 kΩ value of resistor 22 provides a discharge path on this input line to the diode array that protects the array from electrostatic discharge damage when the start pulse circuitry is disconnected.

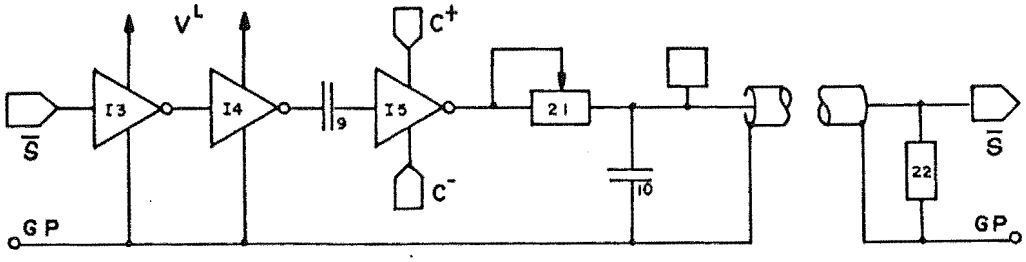


Figure 6.5: Electronic circuit used for conditioning the start pulse control signal.

6.2.4 The Clock Drivers

The master clock, C_m, for each shift register is used by the circuitry given in figure 6.6 to produce the complementary ϕ_1 and ϕ_2 clocks. In doing so, it also gives the required relationship between the edges of the two clocks, as shown by the waveforms in figure 6.7 for the various nodes in the circuitry.

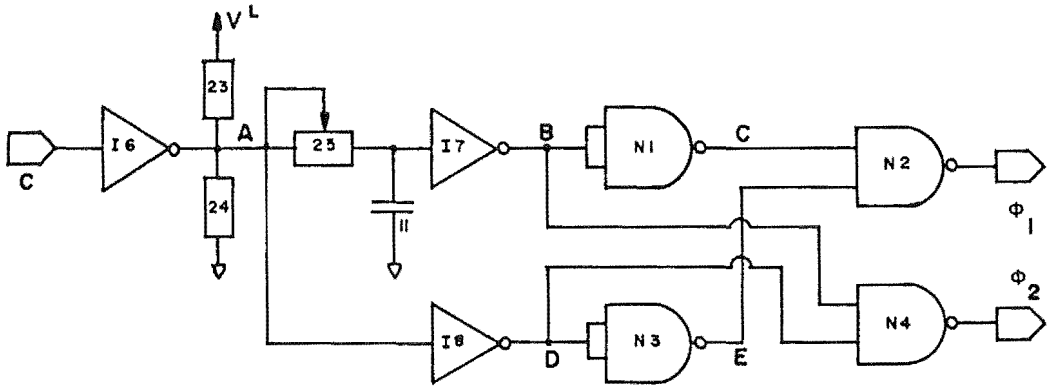


Figure 6.6: Electronic circuit used for producing clock waveforms ϕ_1 and ϕ_2.

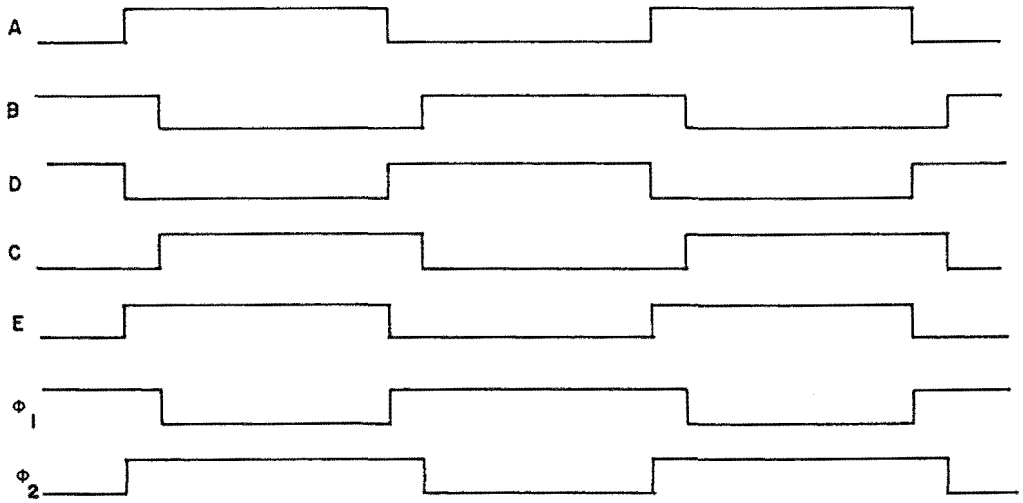


Figure 6.7: Waveforms generated at the nodes shown in figure 6.6.

The ALS invertors I6, I7, and I8 are used with resistors 23, 24, and 25, and with capacitor 11 to produce a time delay between otherwise identical waveforms on nodes B and D. This delay is adjusted to be equal to the required separation in time between the edges of ϕ_1 and ϕ_2, and is

determined by the time constant of the RC network formed by variable resistor 25 and capacitor 11. The output voltage swing of I6 is set with the level translator formed by resistors 23 and 24. The values of these resistors are as low as is practical, and are set so that the same time delay applies to both the rising and falling edges at node B. Inverter I8 balances the propagation delay to node D with that of I7 to node B, and the four ALS NAND gates use these two signals to produce ϕ_1 and ϕ_2 as shown using both figures 6.6 and 6.7. The result is that ϕ_1 rises before ϕ_2 falls, and ϕ_2 rises before ϕ_1 falls. This ensures that during the readout sequence, diode number n is completely turned off before diode n+1 is turned on.

For this circuit to perform correctly it is essential that ALS logic is used for the following reasons. The logic high level of I6 must drive the large output current required by the load of resistor 24, and resistor 25 in series with capacitor 11. The very low input current of I7 allows a high value of 500 Ω to be used for resistor 25 while a logic low is maintained for the input signal level. Also the high value of the threshold input voltage of I7 ensures that resistors 23 and 24 can be selected so that the propagation delay through the RC network and I7 is the same for both rising and falling edges. Finally, the output current capabilities of N2 and N4 are sufficiently high to drive the electronics which condition the clocks for application to the shift registers.

The circuitry which is used to condition each clock is given in figure 6.8. Two DS0026 MOS drivers translate the signal levels from the edge conditioning circuitry to the levels required by the shift registers. They are ac coupled to that circuitry with capacitors 12 and 13. One of those capacitors is a 6.8 μF metallized polyester non-polarized

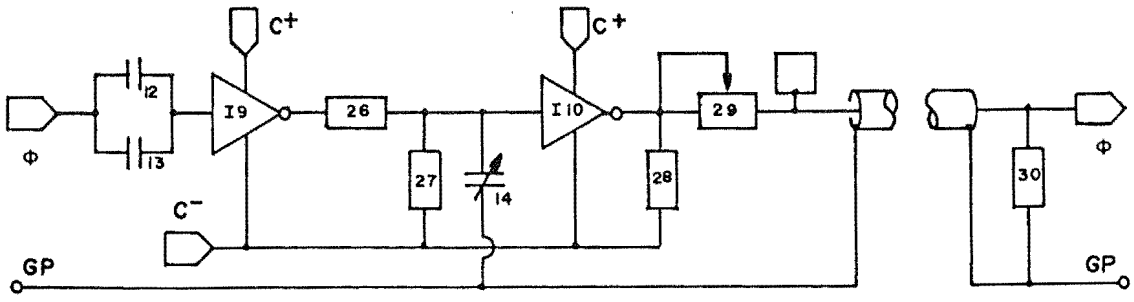


Figure 6.8: Electronic circuit used to condition each clock.

capacitor which passes the low frequency components of the input signal, and the other has a 100 nF value in order to pass the components which are above the frequency at which the 6.8 μF capacitor becomes self-inductive.

The purpose of using two MOS drivers, as suggested by Tull (1982), is that the temperature coefficient of the net propagation delay becomes the same for both rising and falling edges. This occurs because for both types of transition, both a rising and a falling edge are used in their generation, and therefore the different temperature coefficients for the propagation delays of those edges cancel out. Thus if both ϕ_1 and ϕ_2 are generated with the same circuitry, the delay between their pairs of edges will be much less strongly dependent on temperature.

The two MOS drivers are dc coupled together with the level translator formed by resistors 26 and 27. Their net output resistance can be used with optional capacitor 14 to provide an additional propagation delay to the one provided by the edge conditioning circuitry. However the delay is different for the two edge types and so it would not be used in future designs. Resistor 28 is used to ensure that the two MOS drivers provide a constant load on the power supplies, and therefore that power supply common-impedance coupling is minimized between the complementary clocks which share the same supply. This is achieved by resistor 28 having a value which provides the same load to I10, when it is in a logic high state, as is provided to I9 by the series combination of resistor 26 and 27 in parallel with the input impedance of I10.

Variable resistor 29 is used with the diode array clock line capacitance to bandwidth limit the output noise of each clock, while still allowing the fastest possible transition time. Resistor 30 acts as a discharge path to prevent electrostatic discharge damage to the shift register when the diode array clock lines are disconnected from the clock driver electronics.

6.3 Hardware Implementation

The reset and control logic conditioning electronics, and their precision power supplies, are located on the printed circuit board whose layout is given in figure 6.9, and which is shown in plate 6.1. The circuitry for the positive and negative precision voltage references are located above the line receivers at the bottom of the board. The circuitry related to the reset switch logic is located up the centre of the board, and the circuitry for the odd and even shift registers are on its left and right side respectively. For these three areas, the resistor divider networks lie across the board above the main power and control signal interface area, and the precision power supplies are above them again. The actual signal conditioning electronics lie in the top region of the board.

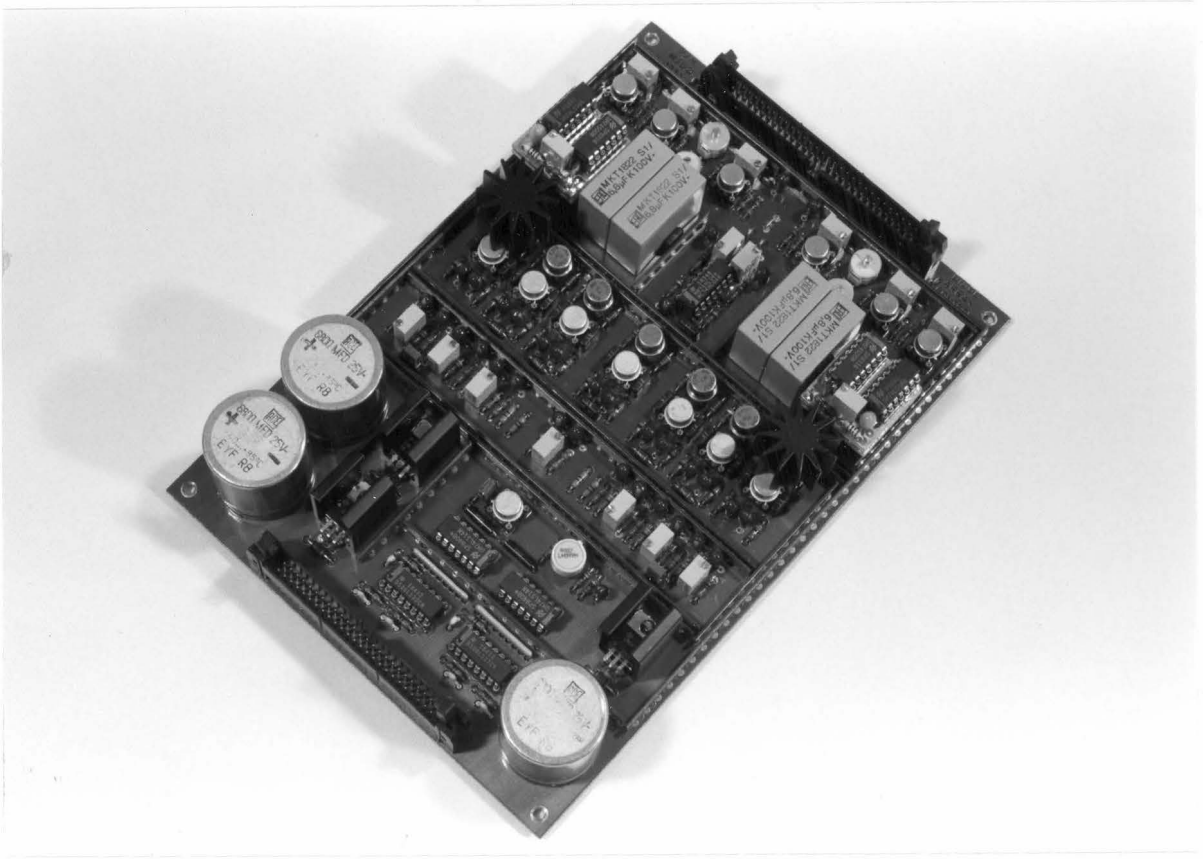


Plate 6.1: The diode array controller board.

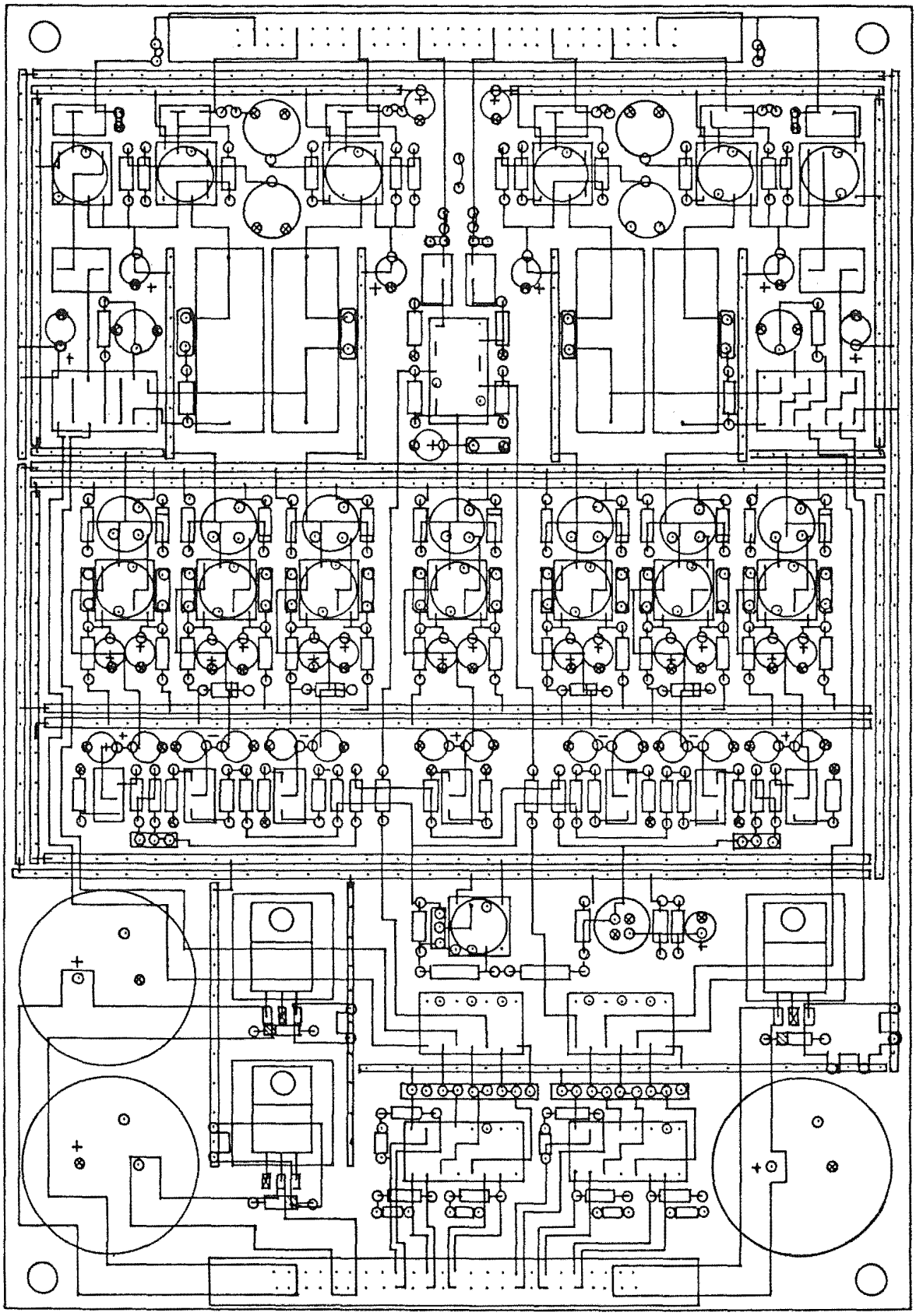


Figure 6.9: Printed circuit board layout for the reset and control logic conditioning.

The edge conditioning circuitry for the shift registers is located on the jumper boards beside the unpolarized capacitors. The boards plug into the dual-in-line sockets seen in figure 6.9, which are from an initial unsuccessful attempt at edge conditioning.

The eight output signals go through the flange to the preamplifier board as described in section 4.1.3, and their routing can be seen on that board in figure 5.4, and in appendix 11. The reset logic lines are distributed to the reset switches along the bottom side of the bottom board so that they are fully shielded from the video lines and preamplifier circuitry. The reset logic pin of the reset switch socket connects the reset switch on the top board to the reset line on the bottom board.

6.4 Performance and Operating Parameters

The difference between the video processing noise and the net readout noise with the diode array was found in section 5.6 to be solely equal to the diode capacitance thermodynamic noise. It follows that the noise contribution from the clock driver electronics must be negligible. Because the reset logic noise couples to the video line with similar mechanisms to the clock noise, it follows that the noise contribution from the reset logic must also be negligible.

The above performance is achieved with clock voltages of +5 and -4.45 volts, which are the values which have been found to give the lowest readout noise. The 9.45 volt amplitude is lower than the minimum value of 11 volts that is recommended by EG&G Reticon for these arrays. This is probably because the recommended amplitude is for applications in which the array is frame read at very high frequencies, whereas the current application is at very low frequencies.

The rise and fall transition times between the traditional 10% and 90% limits are approximatly 12 ns. The offset between the edges is such that the rising edge has reached 95% of its full amplitude when the falling edge has fallen 5% from its upper limit.

CHAPTER SEVEN

DATA ACQUISITION AND REDUCTION

An interface to the system must exist through which the user can flexibly control the detector and its acquisition of image frames, and through which those frames can be processed, displayed, and stored. These tasks are to be performed by the Data Acquisition sub-system, and so the construction of its hardware, and the formulation of the user's interaction with that hardware must be undertaken.

7.1 The Data Acquisition System

The data acquisition system is a microprocessor based computer that has been assembled from vendor and custom sub-systems. The appropriate considerations of assembly or design for those sub-systems, and their organization, function, and performance will now be considered.

7.1.1 The Microprocessor Chassis

The hardware contents of the microprocessor chassis perform the computing and control functions for the Data Acquisition System.

a) The Hardware Organization

The electronic hardware is contained within a standard 19 inch rack mounting electronics chassis of 5 rack units height, and 425 mm X 450 mm internal dimensions. All seams and joints of the aluminium chassis are conductive to ensure moderate suppression of the EMI generated by the processor. The chassis is internally subdivided into two compartments to correspond to the physical organization of the electronic hardware. As shown in plate 7.1, the microprocessor electronics are within one compartment, and the power supply for those electronics is within the other compartment. The organization and operation of the electronics within each of

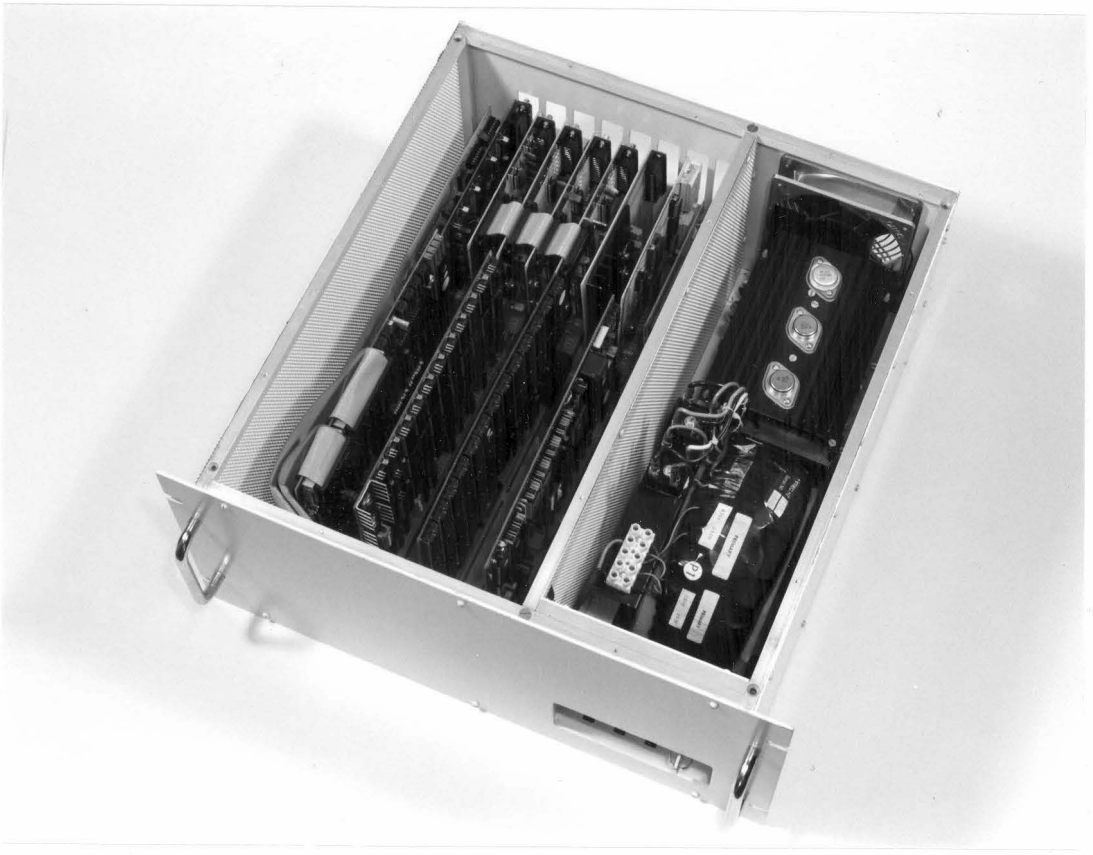


Plate 7.1: The Data Aquisition System microprocessor chassis.

those compartments is as follows.

1) Power supply: Utility power enters this area and is pre-regulated into the power supplies of +8, and ±18 volts potential that are required for the microprocessor electronics. The current capacities of those supplies are 10 amperes, and 5 amperes each respectively. The utility power line is filtered to prevent EMI from being conducted out of the processor chassis, and has a transient suppressor to absorb power transients being conducted in on it that could disrupt the operation of the electronics. External devices can be supplied with utility power from a connector on the back panel of the chassis. Those devices will always turn on and off simultaneously with the processor electronics because they share the same key switch and protection fuse.

2) The Microprocessor electronics: The framework for these electronics is a bus structure which interconnects their sub-systems, that is located on a 'mother-board'. Two buses

are used, which are the 50-way SS-50C and 30-way SS-30C buses developed by Southwest Technical Products Inc. for Motorola 6800 series devices. Eight slots are provided for connecting electronic sub-systems onto each bus, with the SS-50C bus hosting the microprocessor and tasks requiring the full processor control structure, and the SS-30C interface bus hosting the architecturally limited interfacing tasks. As shown in plates 3.8 and 7.1, connectors on the interface boards can be accessed through the back panel of the chassis for connection to external devices. The SS-30C bus is interfaced to the SS-50C bus by an interface driver board located across the top of each bus and along the edge of the mother-board. It also provides general system interfaces including a MC6840 programmable timing module, a baud rate generator for the SS-30C bus, a parallel port, a 'jiffy' counter, and a 50 Hz oscillator locked in phase with the utility power. The pre-regulated power supplies are connected to the mother-board and distributed via the buses.

Both the external wall of the processor compartment and the internal sub-division wall are of perforated metal construction, which allows a fan in the back wall of the power supply compartment to draw air through the entire chassis to cool those components dissipating power.

b) The CPU and Memory

A Motorola MC6809 microprocessor operating at 2MHz controls the Data Acquisition System from a GIMIX 6809 CPU PLUS #5 board on the SS-50C bus. The MC6809 has an 8-bit data path from the internal 8 or 16-bit architecture, and a 16-bit address path which will linearly address 64 kbytes of memory. The operation code set of this processor efficiently supports the implementation of high level languages that use position independent code. The CPU board includes a real time clock and a 1 kbyte scratch pad RAM which are battery backed up, a 2 kbyte EPROM containing the (now modified) GMXBUG monitor firmware, a 2 kbyte EPROM containing the AUTOBOOT software that is used to load the DOS, a Motorola MC6840 programmable timing module, and provision for an arithmetic processor. The board also includes the GIMIX enhanced dynamic address

translator, hereafter the DAT, which increases the amount of memory that the processor can address to 1 Mbyte. This feature allows large application programmes to be executed if they are appropriately implemented. The DAT treats the 64 kbyte address space of the processor, called the logical address space, as 16 linear blocks of 4 kbytes each. It similarly treats the 1 Mbyte address space of the physical memory as 256 blocks of 4 kbytes each. The DAT operates by allowing the user software to map any of the physical blocks of memory into any of the logical blocks of address space in which the processor can address. This allows the processor to address a maximum of 64 kbytes of memory at any one time.

The system memory is supplied by a GIMIX RAM #72 board on the SS-50 bus which provides 256 kbytes of CMOS RAM that operates without wait states or cycle stretching at the 2MHz CPU speed. The RAM is battery backed up which provides 300 hours of data retention after the power has gone down, a feature which will protect data that has not been stored on a permanent medium prior to a power failure. Low voltage detection circuitry on the board also protects memory during power-ups, power-downs, and failures, by inhibiting writes to the memory during those intervals.

c) The Peripheral Interfaces

The processor controls the peripheral devices in this acquisition system with the following two types of interfaces.

1) The disk controller: Floppy disk drives are interfaced by a GIMIX #68 direct memory access (DMA) disk controller board that uses MC6809 cycle steal DMA to transfer at the full 2 MHz bus speed. It will control up to four drives which can be any combination of 5.25 or 8 inch sizes, 3 ms or greater track-to-track stepping speeds, and single or double sided, single or double density storage formats.

2) The serial ports: Peripherals which support the RS-232C communication protocol are interfaced to the processor through a port on one of two SS-30 bus dual-port serial boards. Each port uses an MC6850 asynchronous communication interface adapter (ACIA) chip and provides jumper selectable baud rates between 50 and 38,400. Interrupt requests can be

supplied to the processor by each ACIA when a character has been received and or when the ACIA is ready to transmit another character.

7.1.2 The Peripherals

The peripherals perform the function of interfacing the user to the Data Acquisition System. They are installed with individual utility power lines and communication links between the processor and each peripheral in a 'star' distribution pattern that will enhance the electro-magnetic compatability of the Data Acquisition System.

a) The Terminal

The terminal is comprised of a high resolution RolandDG type MB-142 character display being driven by an Elcoma Terminal Board #1 kitset terminal and keyboard. The terminal architecture is table driven and gives 80 columns by 24 lines, the standard character attributes of the Signetics terminal chip set used, and two intensity levels. Both the hardware and software have been considerably enhanced to support the software that controls the detector. Those enhancements fall onto three areas.

1) The custom character generator: The SCN2670 character generator chip in the Signetics chip set has been replaced by a custom character generator board which plugs into the 2670 socket. It incorporates two 16 kbyte EPROMs to implement fourteen character sets of 64 characters each, in addition to the standard set of 128 ASCII characters. Every character font within the 15 character sets is an array of 9 by 12 pixels, and each pixel in every font can be specified as either on or off, allowing the creation of any character font desired. An interactive DOS utility named FONT has been written to create and edit the custom characters contained within the data files that are programmed into the EPROMs.

2) The wide screen RAM: The random access memory that contains the table of 1920 characters that are displayed on the monitor has been widened from 1 byte to 2 bytes per entry. This allows every character position on the monitor to display

the character specified in the first byte with the attributes specified in the second byte. This has enabled a graphics capability of 240 X 144 pixels to be achieved by the use of multiple custom character sets.

3) Software enhancements: The terminal software has been considerably enhanced to support the character sets of the custom character generator, to implement the wide screen RAM hardware, and to expand the set of software callable commands. One command supports screen-editing user software by allowing any specified rectangular area on the screen to be cleared. Another set of commands allows the processor to temporarily interrupt one task it is writing to the screen by instructing the terminal to store its current status. The processor can then write a second task elsewhere on the screen before restoring the terminal status to complete the first task. This feature allows real-time information to be updated on the screen as a background task to the normal execution of a programme.

b) The Disk Drives

Three disk drives are interfaced to the processor through the disk controller board. Two of those are half-height Shugart SA860 8-inch double-sided double-density drives which support 3 ms track-to-track stepping. They are installed side-by-side and horizontally within a standard 19 inch rack mounting electronics chassis of 2 rack units height, and have an appropriate power supply in the back section of their chassis. A formatted diskette in these drives has 3952 storage sectors of 256 bytes each, and a standard directory size which will hold 250 directory entries. If the directory is extended with the DOS utility EXTEND, a maximum of approximately 475 detector frames can be stored on each diskette.

The third disk drive is a Mitsubishi Electric Corportation M4853-112U 5.25 inch double-sided double-density drive of 3 ms track-to-track stepping time. It is installed within a portable case and receives its power from a power supply board on the SS30 bus. A standard formatted diskette in this drive will have 2844 storage sectors of 256 bytes

each, and a directory which will hold 160 directory entries.

c) The Printer and Plotter

Both the printer and plotter are interfaced to an RS-232 serial port and communicate with the processor at a baud rate of 9600. Their individual descriptions and features of significance are as follows.

1) The printer: This is a C. Itoh & Co. Model M-8510 dot matrix impact printer with a normal printing speed of 120 characters per second. This printer offers a significant number of software selectable features which govern its printing format, and a 2 kbyte input buffer which minimizes the processor time spent on small printing tasks to that of the transmission time.

2) The plotter: This is a Kanto Denshi Corporation KDC-2000 X-Y plotter operating on the friction roller drive principle. It has an effective plotting area of 380 mm X 270 mm, a pen speed of 200 mm s^{-1}, a 5 character per second writing speed, 4 selectable pens, and accepts commands in the Hewlett-Packard graphics language. It features a 500 byte input buffer, 0.025 mm plotter steps, and a repetition accuracy of 0.3 mm.

7.1.3 The Detector Interface

The task performed by this interface was determined in Chapter 3 to be the acquisition of the detector data and status information, and the generation of the system control signals in a manner which would allow them to be readily altered if required. The design and implementation of the interface within the context of the electromechanical design was also determined within Chapter 3, and so the design and implementation of the interface itself must now be determined.

a) Requirements

The functional forms with which the control waveforms must be generated were developed in Chapters 5 and 6. Specifying those waveforms implicity made the following

assumptions, which the waveform generating electronics must satisfy.

1) All the waveforms stay in synchronization with each other as they evolve in time,
and 2) the waveforms can be started up with differences in their relative phases.
Additionally, the control waveforms must be able to operate independently so that the thermometers and temperature controller can be accessed without activating the video processing or diode array control signal conditioning electronics. To fulfill these requirements, and that of allowing simple waveform modifications, Advanced Micro Devices (AMD) Am9513 system timing controller (STC) chips are used to generate the waveforms with some of the techniques specified by AMD (1984). These devices support operation in a microprocessor orientated system, and provide capabilities which include the generation of high temporal resolution programmable duty-cycle waveforms, and complex pulse-packet waveforms. Each STC has five counters which can independently generate a programmable waveform, as described in those parts of the introduction and functional description reproduced in appendix 8 from AMD (1984).

b) Hardware Implementation

Four printed circuit boards on the SS-30 bus provide the interface of the acquisition system to the detector electronics. A single STC is located on three of the four boards, with each of those boards supplying the signals to one interface chassis, and therefore to one of the three dewar electronics boards. To ensure the required sychronization between the waveforms from the three STCs, a 5 MHz quartz crystal oscillator located on one of the STC boards is used to clock all three STCs. That clock is distributed to the other two STCs in the ribbon cable shown interconnecting the boards in plate 7.1, and can be started and stopped with software commands. The waveforms generated on each of the STC boards are given in table 7.1, and indicate that the signal REV must be distributed through the ribbon cable from board #3 to board

Table 7.1: Waveforms generated by the counters of each STC.

	STC1	STC2	STC3
Counter #1	SO	SHR	ADC_e
Counter #2	CO	SHP	PL
Counter #3	ROV	M1	SC_e
Counter #4	CE	M2	DAV
Counter #5	SE	REV	FREE

#2. The three signals T, A1, and A2 required by the A/D convertor and temperature controller board are coupled to the interface chassis of that board from STC board #2. Their logic level is required to only change under software command, and therefore the software writes the required values to that board which latches them for subsequent continuous output to the detector interface chassis.

The fourth interface board receives the serial A/D data and power supply status information from the interface chassis. The serial data is clocked into a sixteen bit serial to parallel shift register by the negated ADC_e signal, as described in section 5.6.2. The control signal is connected from its source on STC board #2, via the ribbon cable, to the shift register. The parallel data is then read from the register by software through a MC6820 Peripheral Interface Adapter (PIA) when the DAV signal is a logic 'true'. That signal is connected to the PIA from its source on STC board #2 via the ribbon cable, which enables it to be read with software. Similarly, the three power supply status lines can be latched and read by software, and can also generate a processor IRQ interrupt via the PIA if an error condition is displayed by any combination of those lines.

Custom hardware was not required to control the relays in the Utility Power Switching chassis because the PIA on the interface driver board was available for generating their control signals.

c) Software Implementation

All the control waveforms generated by the STCs are one of the four modes D,I,J, or Q whose descriptions are reproduced in appendix 8 from AMD (1984). In all cases the counter source is the 5 MHz oscillator allowing the waveforms to be programmed in 200 ns bins, and the output is the terminal count toggled waveform. The waveforms are synchronously started by turning off the oscillator, programming and arming all the counters, and then turning on the oscillator again. That start of each readout is sychronized to the positive going zero voltage cross-over of the utility power supply so that any 50 Hz EMI in the image frame will become a component of the fixed pattern which can be eliminated. During the programming of the STCs, those waveforms which are to have a non-zero phase at the start of their generation, must have that phase entered into their counters. This is achieved by writing the phases into the load registers, loading them into their counters, and then loading the appropriate values which determine the duty cycle

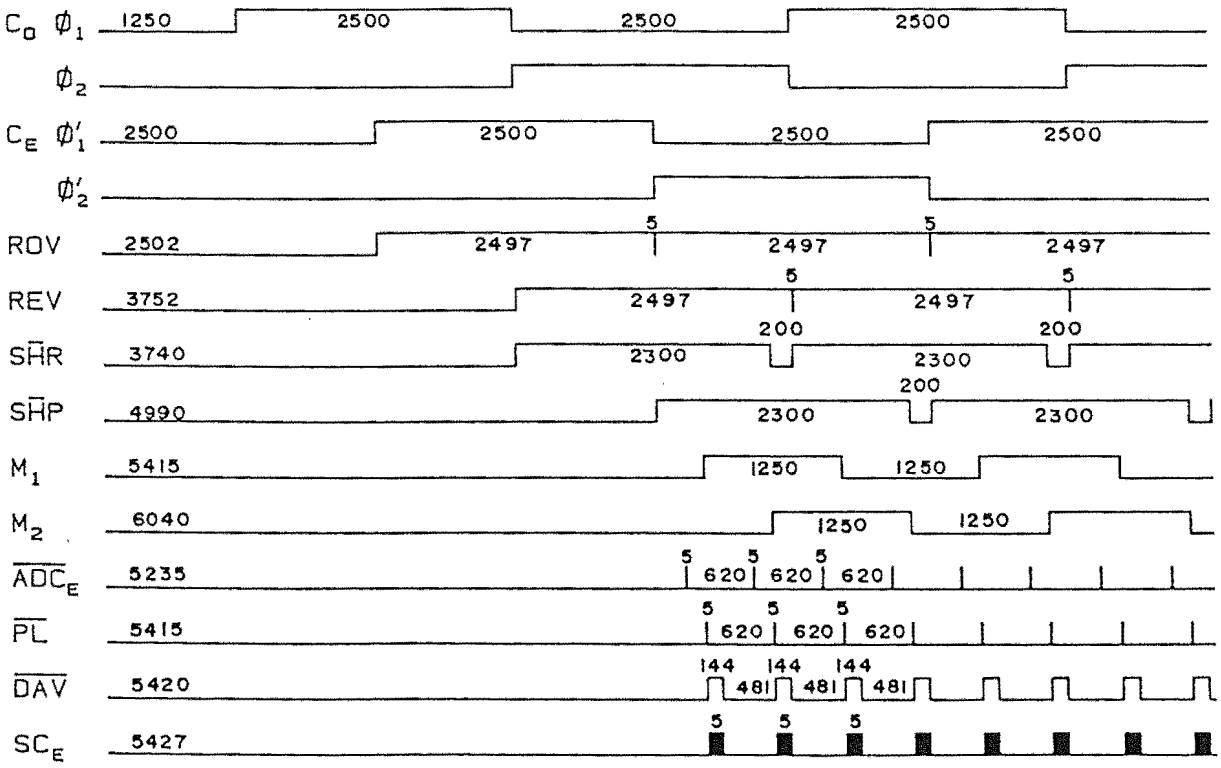


Figure 7.1: Waveforms, as generated by the STCs, for controlling the MJUO LDA.

and period of the waveforms into the Load and Hold registers. Therefore when the oscillator is started, the phase value in the counter determines the first interval until the terminal count, and then the Load and Hold registers determine the subsequent intervals depending on the counter mode. The phase, load, and hold values in units of the 200 ns programming bins are given for each wavefrom in figure 7.1, as are the counter modes. The waveforms are shown as logic level versus time, with the time origin indicating the start of the oscillator, and the logic levels being those generated at the STCs.

7.1.4 The Disk Operating System

A single user DOS is required so that the detector control software can have uninterrupted access to the processor for the real-time task of data acquisition, and therefore the FLEX command line structured DOS produced by Technical Systems Consultants has been implemented. This DOS has an 8 kbyte memory-resident core that performs all the tasks necessary to execute and support any disk-resident utility selected by the command line. Those utilities perform all the user selectable system operations, and include user written programmes. The system utilities of significance to the detector control software include the screen editor, native code Pascal compiler, relocating assembler, linking loader, and debugger, as well as the file management utilities.

7.2 The LDA Control Programme

A programme composed of both assembly language and Pascal modules has been written to control the MJUO LDA detector. The Pascal modules are compiled to form assembly language modules, and all the assembly language modules are assembled and linked together with the required Pascal runtime libraries to form an executable binary file. One general principal applied to the writing of the software is that the programme framework and data reduction tasks would be written

in Pascal, while tasks which control hardware or require speed would be written in assembly language. The organization, operation, and contents of those modules is the subject of this section.

7.2.1 The Software Environment

a) User Interaction

The user controls the system from the terminal by responding to the interactive, information window orientated, menu driven LDA programme. The format of the information displayed on the monitor is shown in plate 7.2, which is composed of the following six information windows.

1) The real time information line: this line is updated each second, and provides universal time, the array temperature, the temperature controller power, the observatory air temperature, and the detector integration time.

2) The system status: this window displays the status of the detector power supplies, the reference temperature at

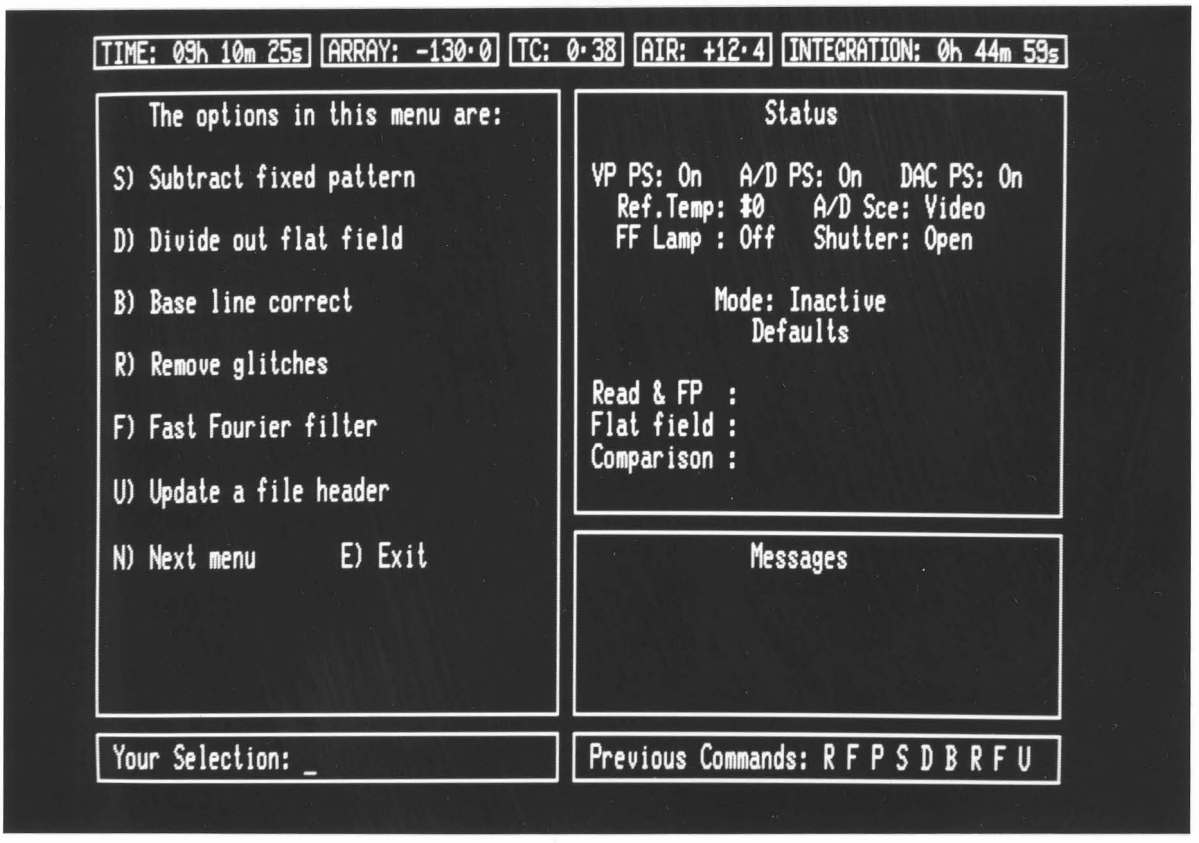


Plate 7.2: General operating format of the LDA programme.

which the array is being controlled, the input source to the A/D convertor, whether the flat-field lamp is on or off, and whether the shutter is open or closed. It also displays the mode in which the detector is being run and has provision for default values for automatic modes of operation.

3) The options menu: the menu of options available to the user is displayed here. The user responds at the appropriate time with the letter of the option to be performed. At least one option in any one menu allows the user to enter another menu. The principal menus are for observing, data processing, data displaying, data storage and retrieval, and testing of the detector hardware.

4) Command Selections: commands and additional information are prompted for within this window.

5) The message window: warnings, error messages, and numerical information about data reduction tasks are displayed here as they occur.

6) The previous commands: the calling letter of the ten most recently executed tasks are displayed within this window to support the user's memory while performing a sequence of events.

b) The Runtime Environment

The following two aspects of the software runtime environment are deviations from a normal configuration which dominate the structure of the assembly language software.

1) The task of supplying the real time information to the user terminal is performed under interrupt control so that its execution is transparent to the normal command and response interaction of the programme with the user. That background task uses a negligible 0.1% of the total processor time, and a just perceptible 5.6% of the output time to the terminal.

2) The combined size of the programme code, user variable storage space, and the runtime data stack is larger than the amount of free memory in the logical address space of the processor. Therefore the programme has been implemented using the DAT to extend the available memory. Programme procedures and image frame storage buffers are mapped into the logical

address space only when they are required for execution or processing. Only the data stack, runtime libraries, abort routine, and code supporting the real time information line are mapped into the logical address space continuously because they are required at all times.

c) The Image Frames

Each image frame is stored as a Pascal RECORD data structure of the format given in figure 7.2. The format has two principal components, the header, and the data buffer. As shown, the data buffer is an array of either 936 or 1872 16-bit integers, a format compatible with the 14-bit data generated by the detector A/D convertor.

The header contains a full set of information about the observation. The array size and mask positions are automatically entered at the time of readout, and are the sole specification of those parameters for any routine that subsequently handles or processes the frame. The values which are entered can be updated using the DOS utility MASKS whenever the mask is moved. The first and last pairs of positions delimit the short and long wavelength regions, respectively, which are partially shadowed by the ends of the mask. The information inclusive of the date and base line value are also automatically recorded, either at the time of readout, or during the following data reduction. The remaining details can be entered interactively by the user. Each image frame of this format is saved in 9 disk sectors with a 936 pixel array, and in precisely 16 disk sectors with a 1872 pixel array.

Six image frames are used within the programme, their names are Raw Data, Fixed Pattern, Data, Flat Field, Spectrum, and Thorium Lamp.

7.2.2 Detector Control Software

a) Readout Software

Software written in assembler is called from the main

```
TYPE
  buffer_type = ARRAY  [1..max_array_size ] OF integer                    ;
  date_type   = RECORD
                  day      : byte ;
                  month    : byte ;
                  year     : byte
                END ;
  time_type   = RECORD
                  hours    : byte ;
                  minutes  : byte ;
                  seconds  : byte
                END ;
  header_type = RECORD
                  classification             : hex                        ;
                  array_size                 : integer                    ;
                  mask_position_1            : integer                    ;
                  mask_position_2            : integer                    ;
                  mask_position_3            : integer                    ;
                  mask_position_4            : integer                    ;
                  star_name                  : STRING [10]                ;
                  observer                   : STRING [12]                ;
                  date                       : date_type                  ;
                  start_time                 : time_type                  ;
                  length                     : time_type                  ;
                  array_temperature          : integer                    ;
                  controller_power           : byte                       ;
                  maximum_value              : integer                    ;
                  mean_value                 : integer                    ;
                  flat_field_mean            : integer                    ;
                  scale                      : integer                    ;
                  base_line                  : integer                    ;
                  central_wavelength         : integer                    ;
                  order_number               : byte                       ;
                  seeing                     : byte                       ;
                  slit_width                 : integer                    ;
                  cross_grating_type         : byte                       ;
                  cross_grating_micrometer   : integer                    ;
                  echelle_tilt_micrometer    : integer                    ;
                  echelle_filter             : STRING [5]                 ;
                  slit_height                : integer                    ;
                  slit_position              : integer                    ;
                  camera_micrometer          : integer                    ;
                  collimator_micrometer      : integer                    ;
                  dewar_position             : ARRAY [1..2] OF byte       ;
                  comment                    : STRING [50]                ;
                  Log_zero_frequency_power   : real                       ;
                  Log_Spectral_constant      : real                       ;
                  Log_noise_power            : real                       ;
                  dispersion_0               : real                       ;
                  dispersion_1               : real                       ;
                  dispersion_2               : real                       ;
                  dispersion_3               : real                       ;
                  expansion_area             : ARRAY [1..122] OF byte
                END ; {record}
  array_type  = RECORD
                  header : header_type ;
                  buffer : buffer_type
                END ;
```

Figure 7.2: Software storage format for image frames.

Pascal programme to readout the array, and the resulting image frame can be read into either of the Raw Data or Fixed Pattern image frame. The assembly language software initializes the system timing controllers which generate the detector control logic, and reads in the data from each pixel as described in section 7.1.3.

b) Auxiliary Hardware Control

Within appropriate menus, the user can call assembly language routines which perform the following tasks.

1) Turn the detector power on or off,

2) select one of the two reference temperatures at which the array can be controlled,

3) turn the flat field lamp on or off,

and 4) select one of four possible signal sources to be multiplexed to the input of the A/D convertor for use in the testing procedures.

c) Testing Support Routines

The testing menu previously referred to enables the user to perform the following four tasks that can enable detector parameters to be adjusted, or faults to be diagnosed.

1) Read and display the A/D: individual reads of the A/D convertor can be made for the signal source that has been selected. The result is displayed in the messages window.

2) Calculate the mean readout noise: the average readout noise profile of any combination of video lines is determined and plotted on the printer. This is performed by subtracting one fixed pattern frame from another, and plotting the differences for the selected video lines as an histogram.

3) Continuously operate the detector: the STCs continously operate the detector electronics so that a user can examine the circuitry with an oscilloscope.

4) Frame read the array: the array is readout every second so that an oscilloscope can be used to repetitively display the electronic response of individual readouts.

7.2.3 Data Reduction

a) Fixed Pattern Subtraction

The contents of the data buffer in the Fixed Pattern frame are subtracted from the data buffer of the Raw Data frame, and the user specifies which one of the Data, Flat Field, or Thorium Lamp frames into which the result goes. The Raw Data header is copied into the result frame header, and the mean and maximum value of the result are entered into the result frame header and reported to the user in the messages window.

b) Base Line Subtraction

The additive thermal leakage base line is calculated and subtracted from one of the Data, Flat Field, of Thorium Lamp frames as specified by the user. The base line is calculated as the linearly interpolated line between the measured value of the base line at each end of the array. Each of those measured values is the average of approximately the 12 pixels which are masked from light, as described in section 4.1.3, at each end of the array. The averaging process increases the accuracy with which the base line is known at each end of the array to $\approx 1/\sqrt{12}$ of the readout noise. Long integrations in the absence of light give the base line along the entire array, and have shown that there is no pixel number dependent structure that is detectable in addition to the readout noise fluctuations. The base-line procedure records the average value of the base line and the new mean and maximum values in the frame header, and reports them to the user in the messages window.

c) Flat Field Division

The user can specify that the contents of the Flat Field frame be divided into either of the Data or Thorium Lamp frames, with the resulting frame stored in the Spectum or Thorium Lamp frames respectively. The header of the dividend

frame is copied into the header of the quotient frame, and the maximum, mean, scale factor, and flat field mean values are updated. The pixels on a given video line whose signal is diminished by the base line mask, are divided by the mean of the 8 closest pixels on the same video line within the divisor frame that are not affected by the mask. Any flat field pixels which have a zero signal level are replaced by the mean flat field value of the video line that the pixel is on.

d) Deglitching

The user can specify one of the Data, Flat Field, Spectrum, or Thorium Lamp frames from which to interactively remove glitches such as cosmic ray events. While this routine is not intended for removing noise, the performance of the fast Fourier filtering is enhanced if the ≈5% of pixels whose noise exceeds 2σ are deglitched. The display format of the deglitching software is shown in plate 7.3, and is composed of

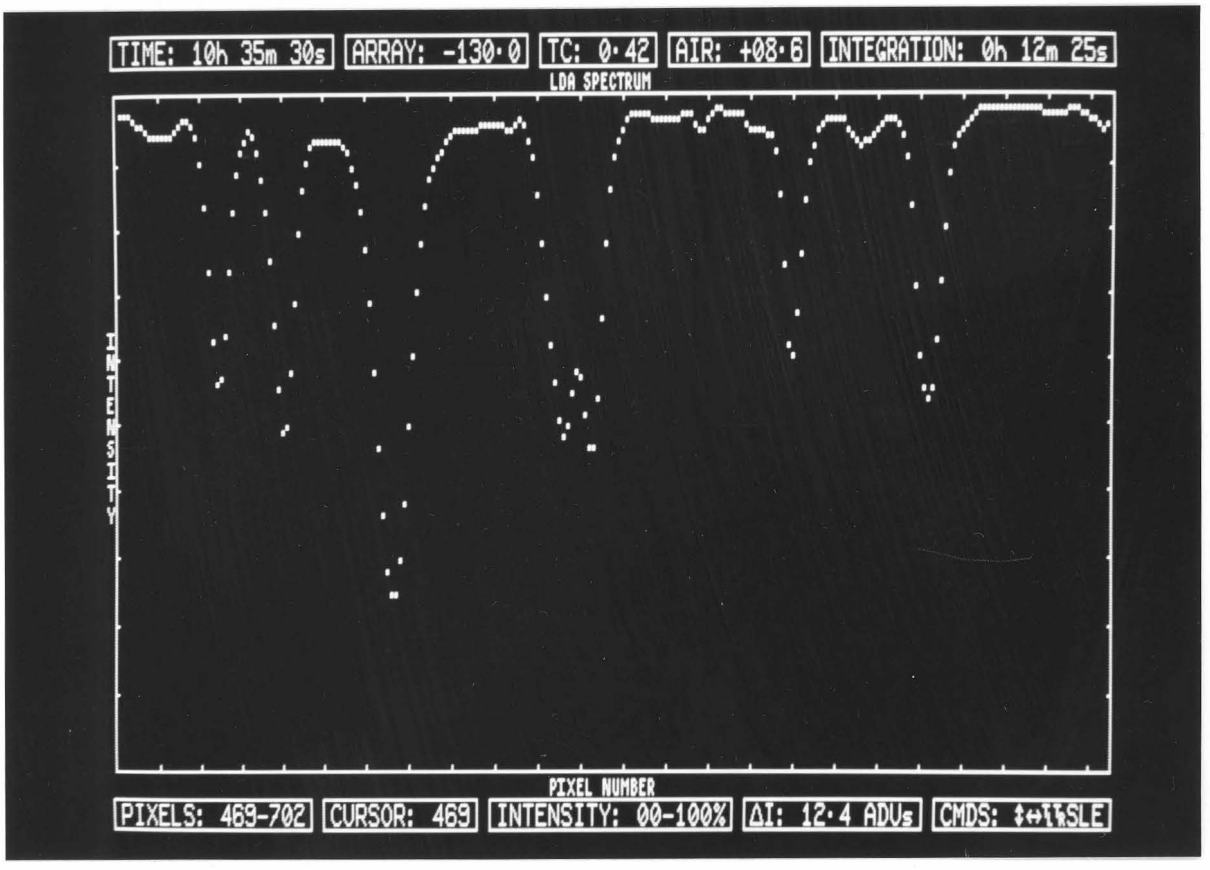


Plate 7.3: Interactive graphics display format of the LDA programme.

the real time information line, a 234 X 120 pixel graphics window, and a graphics status information line. The data from precisely one quarter of the 936 pixel array is displayed at any one time with one of the pixels blinking at a 7.5 Hz rate. That pixel is said to be pointed at, with the pointing function able to be moved along the spectrum to any desired pixel by the use of the keyboard horizontal cursor keys. The pixel being pointed to can be moved up or down the display by use of the vertical cursor keys, with the intensity of the final position being updated in the frame buffer if it has been changed. The horizontal movement of the pointer, and vertical movement of the pixel in response to the appropriate cursor key occurs at a 15 Hz rate when the auto repeat keyboard function is used. Faster horizontal movement can be achieved with the tab right and tab left keys which move the pointer ten pixels per key-press, or at a 150 Hz rate when the auto repeat key is used. Additional commands move to different display pages within the image frame.

The deglitching function is achieved by an interactive interrupt driven assembly language subroutine. Because the terminal is a character terminal, custom character sets were created (see section 7.1.2) to give the 343 different possible characters required to plot a function if each character is considered as an array of 3 X 6 pixels. The custom character sets are given in appendix 9. Because more than one pixel can occur within one character, an algorithm is used to select the appropriate characters. The blinking function is achieved by alternately writing the characters with the required pixel on and off to the terminal, taking into account the other pixels which might be displayed within the same character, and only changing the displayed state of the pixel when signaled to do so by a 15 Hz interrupt. Commands from the keyboard are buffered under interrupt control and are executed when those same 15 Hz interrupts occur. The total calculation and display time for a typical spectrum is $\approx$0.6 seconds.

e) Fast Fourier Filtering

The user can specify either the Spectrum or Thorium Lamp frame to be filtered in the Fourier domain by the optimum

filter of Brault and White (1971). The procedure which performs this task subtracts the data mean, apodizes the data at each end, extends the data array to 1024 points with values of the zero mean, fast Fourier transforms the data, calculates and applies the filter, re-transforms the data, and restores the mean and array length. The parameters of the filter are displayed in the messages window and the option of plotting, and/or listing, the unfiltered and filtered power spectra is given. A sample unfiltered power spectrum, of the spectrum shown in figure 7.4, is given in figure 7.3.

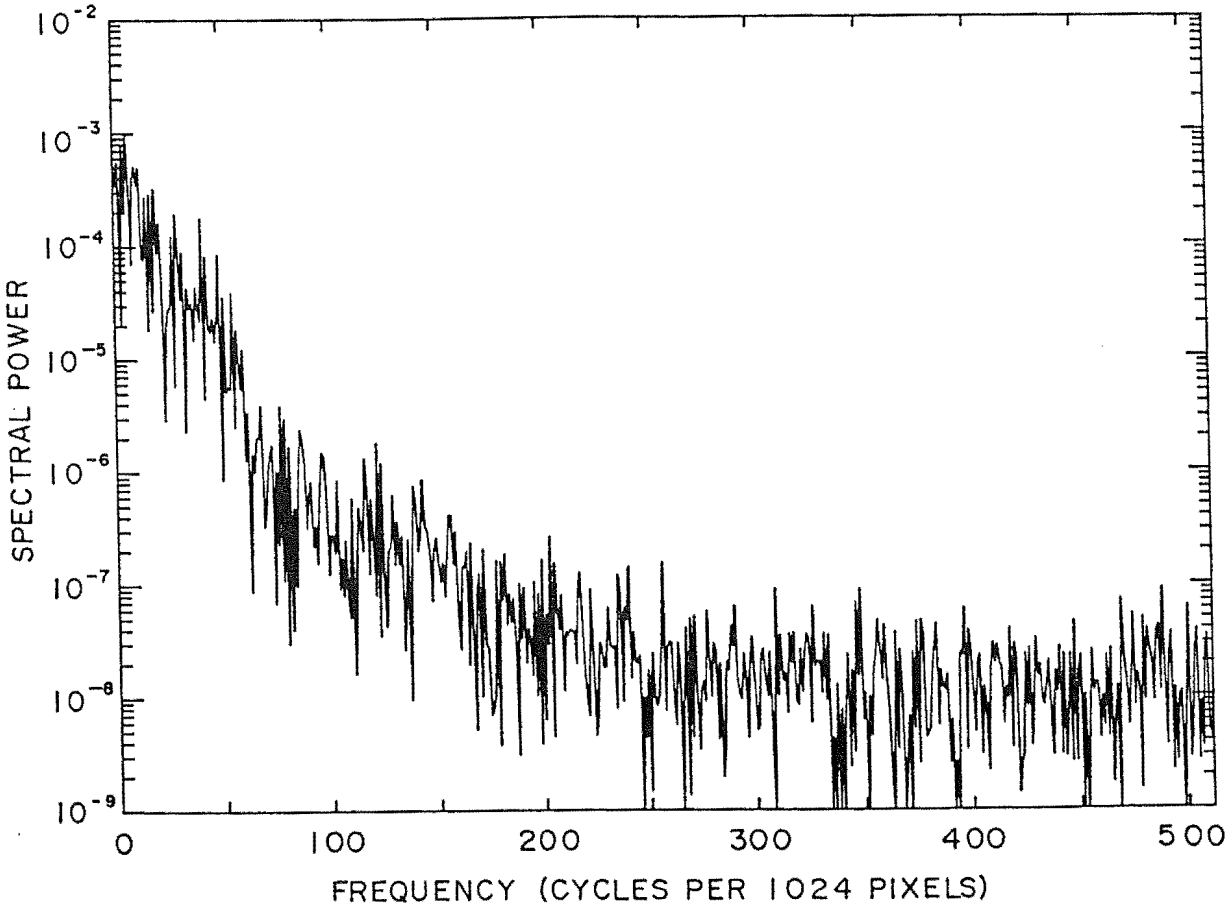


Figure 7.3: Unfiltered power spectrum.

A 1024 point transform requires two 1024-point arrays of real numbers, a total of 8 kbytes of memory in this data acquisition system, of which half is not used if the imaginary component of the input data is zero. Therefore the correct technique is used to load the 1024 input data points into the the real and imaginary arrays of a 512 point transform. This saves memory, increases the execution time by a factor of two,

and allows for upgrading to a diode array of 2048 pixels maximum length because a 1024 point transform is the largest that can be allowed. The execution time of the total filtering procedure is 32 seconds.

f) Dispersion Solution Fitting

The dispersion solution is calculated for the Thorium Lamp frame. The user sequentially enters the short and long wavelength pixel limits of each line to be used in the solution, and the central pixel number of an area of 9 pixels which represent the lamp continuum at the line. The nine pixels are averaged so that the local continuum can be subtracted from the line, and then a Gaussian is fitted between the line limits. The line centroid, FWHM, peak value, and fractional r.m.s. error are displayed to the user in the messages box, and the user can accept or reject the solution. If it is accepted, the user enters the line wavelength which is stored with the centroid until the last line is entered. Then either a linear, quadratic, or cubic solution is fitted to the stored values depending on whether there are two, three, or four or more lines specified. The mean r.m.s. error in mÅ is displayed in the messages box, and is listed on the printer with the solution, line centroids, actual wavelengths, calculated wavelengths, and wavelength errors. The solution is stored in the header of the Thorium Lamp frame, and if the user specifies, also in the header of the Spectrum frame.

7.2.4 Data Display

The user can display the contents of the data buffer and header of each image frame on the Data Acquisition System peripherals in the following ways.

1) The data buffer contents: these can be displayed in graphical form on either the terminal or the plotter. When displayed on the terminal, the same format is used as was shown for the deglitching procedure. The user can specify any sub-range in the 0-100% intensity range of the data to be expanded to the full screen size, and also specify the lowest pixel number of the 234 pixels being displayed. The display

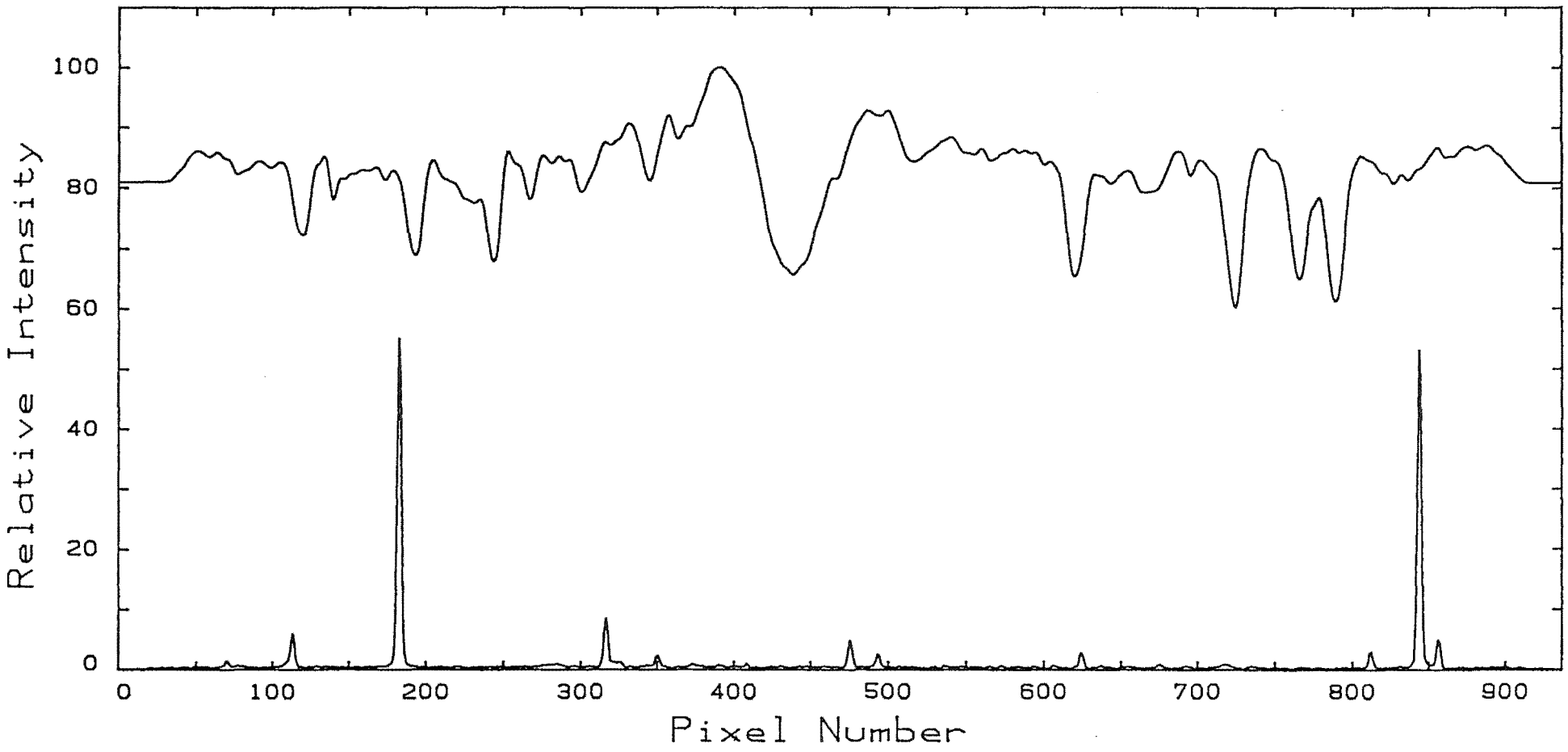


Figure 7.4: Sample plotter output - HR4492 Hα spectrum.

on the plotter has the format shown in figure 7.4, and takes ≈100 seconds to be plotted. The data buffer contents can also be listed in numerical form on both the printer and the terminal. When listed on the printer, the 57.5 lines of 16 pixels fit onto a single page. This is a line format that is useful for testing because every pixel in a given column is on the same video line. The buffer contents are listed in the menu window on the terminal as 13 pages of 72 pixels in a 4 X 18 pixel format. The pixel number of the first pixel in each row is given, and the columns from left to right correspond to video lines 1 to 4.

2) The header contents: these can currently be listed with the format shown in figure 7.5 on the terminal and printer. When listed on the terminal, they appear in the menu window.

SPECTRUM FRAME HEADER

Star: HR4492	
Date: 28/10/85	Obs: PJM
UT: 15h 42m 00s	Length: 1h 15m 00s
Array: 134.0	Air: 7.3
Maximum: 10000	T.C.: 0.42
Mean: 8298	FF mean: 6083
Scale: 11.28	Base Line: -4
λ Region: 6563	Order: 35
Seeing: 2.0	Slit Width: 454
X type: Visual	X micro: 1.4165
échelle: 520	Filter: 0-52
Height: 425	Position: 267.5
Camera: 710	Collimator: 666
Dewar: 29:17	
Comment: File HR4492AA.SPC	
(cont.) Air mass > 2	

Figure 7.5: Display format for an image frame header.

7.2.5 Disk File Operations

It is essential for the user to be able to permanently save new image frames as disk files, and to be able to recover those files at any later stage. It is also highly desirable to be able to manipulate those files from within the detector

programme so that the user has no need to exit into the operating system. While perfoming those operations, it must be impossible for the user to crash the detector programme and therefore the detector. To meet these requirements, the following functions can be performed from the disk operations menu, which are implemented as assembly language routines.

1) Saving disk files: The user is asked for the name the file is to be called, the image frame buffer to be saved, and then whether the task should be executed, aborted, or have its questions re-issued. The drive field in the file name defaults to the work drive, and the extension field defaults to the one of RAW, FPT, DAT, FTF, SPC, and LMP which corresponds to the selected frame buffer. The typical execution time is ≈4 seconds.

2) Loading disk files: The user is asked which image frame buffer the file is to be loaded into, the name of the file, and whether the task should be executed, aborted, or have its questions re-issued. The default values for the file name are the same as above, and the typical execution time is ≈3 seconds.

3) Disk drive directory listing: The user is asked which drive is to be listed, and the file names are listed in pages of format 2 X 16 names. The default drive is the work drive.

4) Renaming Disk Files: The user is asked for the name of the disk file to be renamed, and for its new name. The default values are the work drive and an extension of SPC, and the typical execution time is ≈2 seconds.

5) Deleting disk files: The user is asked for the name of the file to be deleted, and whether the task should be executed, aborted, or have the question re-issued. The defaults are the work drive and an extension of SPC, and the typical execution time is ≈2 seconds.

CHAPTER EIGHT

HR4492: A SOUTHERN RS CVn BINARY

Following the commissioning of the LDA detector system in a laboratory environment, a programme of observational astronomical spectrography was carried out on the southern RS CVn binary star HR4492. One purpose was to determine the performance of the detector system when applied to a task which was typical of that for which it was designed, and the other was to further investigate the programme star. The astronomical information reduced from those observations forms the content of this chapter.

8.1 Introduction

The RS Canum Venaticorum (RS CVn) binaries are a class of close binary systems containing late-type components displaying high levels of surface, chromospheric, and coronal activity which appear to be magnetic in origin. D.S. Hall (1976) has proposed a working definition of an RS CVn binary as one with the hotter component having an F-G V-IV spectral type, an orbital period between one day and two weeks, and strong Ca II H and K emission visible outside eclipse in the spectrum of the cooler component, or in some cases, in both components.

The RS CVn classification of HR 4492 was based upon its classification by Houk and Cowley (1975) as a G5/8 III object with strong H and K emission and suspected photometric variability. Subsequently Stacey, Stencel and Weiler (1980) found some evidence for radial velocity variations based on 40 Å mm^{-1} blue spectra.

HR 4492 (HD 101379) forms a visual binary of 0.24 ± 0.02 arc seconds separation and unknown period (Worley 1981) with the A0 star HD 101380. This companion star is approximately 0.8 magnitudes fainter in the visual photometric band, and is also a binary system. Collier (1982) photometrically determined, from three primary and one secondary eclipses, that its primary and secondary stars are

AOV and A2V respectively, and that their photometric ephemeris is

$$HJD = 2444362.693 \pm 2.7546\ E \qquad (8.1)$$

Collier (1982) also deduced from his photometry that the active component in HR 4492 is of spectral type K4 III, which has a mass and radius of 2.5 ± 0.5 $M_{\odot}$ and 40 ± 10 $R_{\odot}$ respectively, and showed variability indicative of spot waves.

The radial velocity ephemeris given by Collier (1982) for the binary motion of HR4492 is

$$HJD = 2444552.52 + 53.85\ E \quad . \qquad (8.2)$$

It was determined from the metallic photospheric lines in 28 Hα spectra, and the chromospheric emission lines in 7 H and K spectra. The spectra were obtained during seven 1 to 3 day intervals over a period of 3½ years, with 22 of them collected in two of the intervals. His heliocentric Hα data is reproduced in table 8.1 for subsequent use, with only the most representative datum from a given day being tabulated. Their precision is ±3 km s^{-1}. Collier's velocities from his H and K spectra have been disregarded because it has not been demonstrated that a velocity from a chromospheric emission line can reliably represent that of the photospheric lines.

Collier's Hα spectra show that the Hα line profile contains red and blue emission wings, and that the profile varies in time.

At non-optical wavelengths, Garcia et al. (1980) identified HR4492 as the optical counterpart of the UHURU X-ray source 4U 1137-65, after a precise position was obtained with the HEAO 1 scanning modulation collimator. Additionally, Collier et al. (1982) detected it as a strong flaring radio source based on 5 GHz observations obtained with the Parkes 64m radio telescope. During the radio flares, the red emission at Hα was seen to be enhanced.

TABLE 8.1 : Existing Hα spectroscopic observations of HR4492.

UT Date	HJD 244+ (mid exposure)	V_r (kms^{-1})	Phase[a]	Detector[b] & Observatory[c]
27/02/78	3567.04	-4.2	0.94	IT MJUO
08/05/79	4002.00	-3.2	0.88	IT MJUO
07/06/80	4398.05	20.0	0.03	IT MJUO
08/06/80	4398.88	20.3	0.07	IT MJUO
08/06/80	4399.04	20.8	0.07	IT MJUO
08/06/80	4399.12	21.8	0.08	IT MJUO
09/06/80	4399.96	21.1	0.12	IT MJUO
11/06/80	4401.79	18.7	0.20	IT MJUO
29/07/80	4449.94	15.5	0.41	IT MJUO
30/07/80	4450.91	17.5	0.45	IT MJUO
22/02/81	4658.02	8.1	0.94	IT MJUO
23/02/81	4659.04	7.4	0.99	IT MJUO
23/02/81	4659.20	7.8	0.00	IT MJUO
16/07/81	4801.89	-2.8	0.54	PCA MSSSO
17/07/81	4803.00	-2.4	0.59	PCA MSSSO
18/07/81	4803.91	-3.9	0.63	PCA MSSSO
19/07/81	4804.96	-4.9	0.68	PCA MSSSO

[a] Based on new ephemeris given in equation 8.3

[b] IT = Image tube, and PCA = Photon couting array

[c] MJUO = Mount John University Observatory,
MSSSO = Mount Stromlo and Siding Spring Observatory

8.2 Observations

Twenty-four spectra were collected using the échelle spectrograph (Hearnshaw 1977) and 0.61m Boller and Chivens telescope at Mount John University Observatory. They comprised the 19 Hα, 3 He I 5876 Å (D_3), 1 Li 6707 Å, and 1 He II 4686 Å region spectra given in table 8.2.

TABLE 8.2: LDA spectroscopic observations of HR4492.

UT Date	HJD 244+ (mid-exposure)	λ_c (Å)	V_r (kms^{-1})	Phase[a]
11/09/85	6319.839	6563	32.23	0.10
12/09/85	6321.235	6563	28.34	0.17
13/09/85	6321.853	6563	28.85	0.19
13/09/85	6322.237	6563	25.51	0.21
14/09/85	6322.891	6563	26.68	0.24
15/09/85	6323.876	6563	25.85	0.29
8/10/85	6346.860	6563	21.32	0.34
10/10/85	6548.867	6563		0.43
11/10/85	6550.228	5876		0.49
27/10/85	6366.068	6563	23.16	0.22
27/10/85	6366.165	5876	22.59	0.23
28/10/85	6367.104	5876	22.50	0.27
28/10/85	6367.181	6563	23.04	0.27
29/10/85	6368.072	6563	20.61	0.31
29/10/85	6368.164	6707	21.80	0.32
30/10/85	6369.077	6563	19.82	0.36
30/10/85	6369.168	4686		0.36
23/02/86	6484.948	6563	-4.93	0.67
01/04/86	6521.944	6563		0.36
14/04/86	6535.060	6563	4.98	0.97
16/04/86	6536.931	6563	9.15	0.05
16/04/86	6537.119	6563	9.63	0.06
17/04/86	6537.488	6563	9.69	0.08
18/04/86	6538.032	6563	9.77	0.10

[a] Based on new ephemeris given in equation 8.3

A two arc second slit width was used which theoretically projects onto 4.0 detector pixels, which with the spectrograph dispersion of 1.60 kms^{-1} $pixel^{-1}$, gives a resolution of 46,900.

Immediately following each stellar integration, fixed-pattern and flat-field frames were integrated, as was a frame of the thorium-argon comparison lamp in the spectrograph. The stellar and comparison lamp spectra were fixed-patterned and flat-fielded, then the stellar spectra were de-glitched and fast fourier filtered as described in section 7.2.3.

Subsequent to the observational programme, the FWHM of the comparison lamp emission lines were determined by fitting them with Gaussian profiles. A typcial width of 3.0 pixels was found which is inconsistent with the projected slit width of 4.0 pixels. A laboratory inspection of the spectrograph showed that after collimation, the beam from the comparison lamp was a non-uniformly illuminated irregular shape of approximately 10 mm diameter. Incorrectly focussed comparison lamp optics resulted in the slit vignetting the beam from its required 56 mm diameter. The consequence was that the stellar and comparison beams were not illuminating the spectrograph optics in the same way, and therefore that the accuracy with which radial velocities could be determined was systematically degraded. However the precision of those velocities would not be affected, since this is still determined by the traditional sources of that type of error, as discussed by Griffin and Griffin (1973). As a consequence, all radial velocities determined with this spectrograph to date will be systematically inaccurate.

8.3 Analysis

8.3.1 Radial Velocities

A rest wavelength dispersion solution was determined from the comparison lamp frame for each of the spectra, as described in section 7.2.3. Six lines were used in each of the Hα and Li 6707 Å regions, and twelve were used in the D_3

region. Their rest wavelengths were obtained from Chaffee and Peters (1983). The r.m.s. fits of the solutions were less than 2 and 3 mA respectively, which corresponds to approximately 90 and 130 m s^{-1}.

With the exception of the observations at HJD 2446537.488 and HJD 2446538.031, the centroid was estimated to 0.5 pixels for each of the photospheric metallic lines listed in table 8.3 that occurred in a given spectrum.

TABLE 8.3: Spectral lines used for radial velocities.

Wavelength[a]	Identification[a]
5859.594	Fe I
5862.365	Fe I
5866.456	Ti I
5878.800	Ti I
6546.248	Fe I
6554.232	Ti I
6572.784	Ca I
6574.233	Fe I
6575.023	Fe I
6703.572	Fe I
6710.321	Fe I
6713.049	Fe I

[a] From Pierce and Breckenridge (1973)

The individual geocentric radial velocities of those lines were determined using the dispersion solution, and then averaged before being converted to the heliocentric velocities given in table 8.2. The internal precision of a typical spectrum, as determined from the scatter in the velocities of individual lines, was 0.6 km s^{-1}. The precision of the velocity determined from a typical spectrum can be found from figure 8.1. It shows the seven radial velocities as a function of time that were determined between HJD 2446366.07

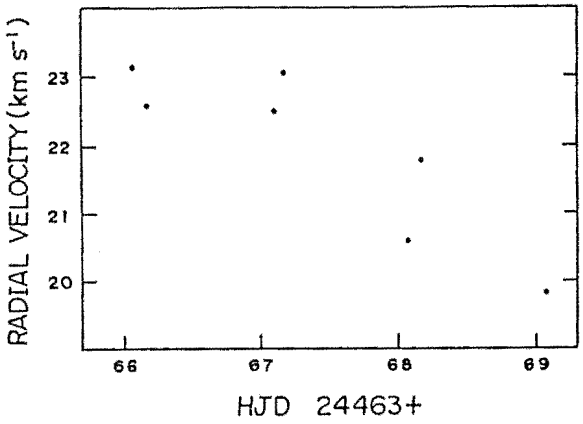


Figure 8.1: Radial velocity versus Julian Date, showing the precision of the velocity determination.

and HJD 2446369.08 in three spectral regions. The precision is seen to be better than about ±0.5 km s^{-1}.

An attempt was made to refine the binary orbital ephemeris in equation 8.2 by plotting the velocities in tables 8.2 and 8.3 modulo orbital phase. The result is given in figure 8.2, which shows that the ephemeris cannot account for the new observations. Inspection of a velocity versus time

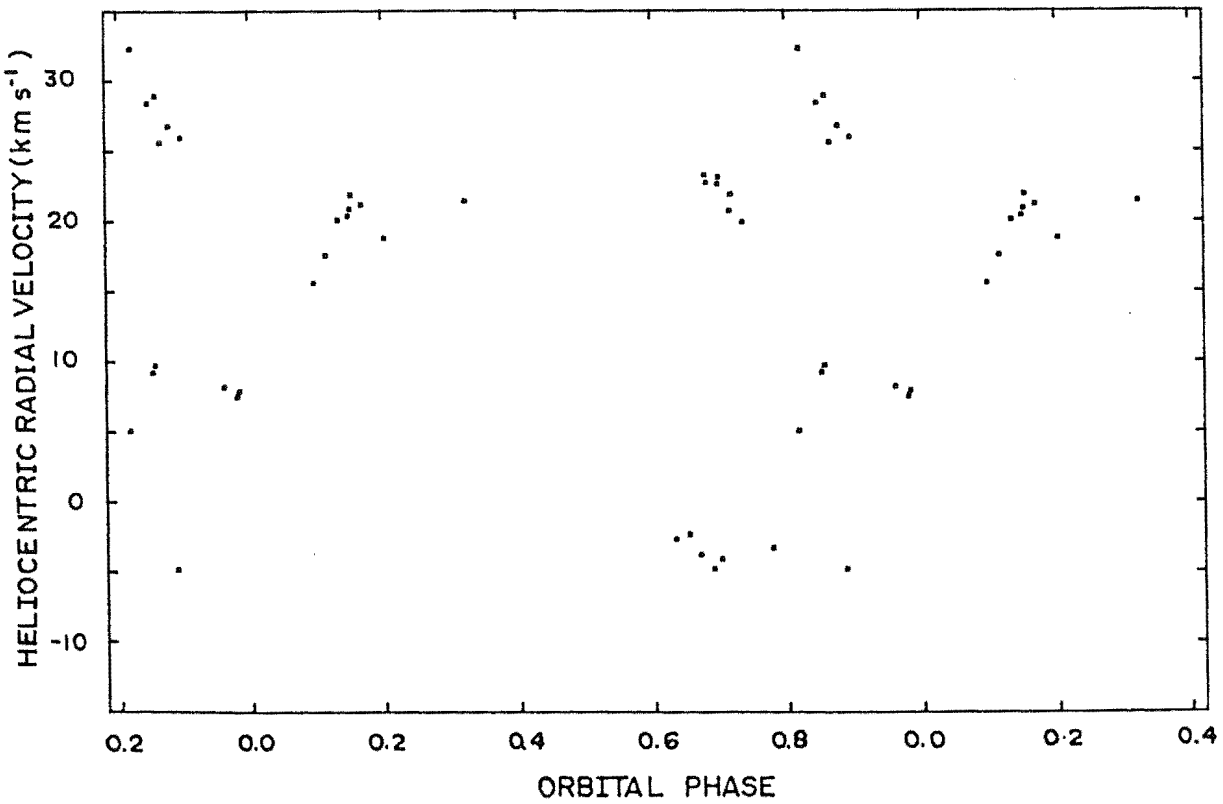


Figure 8.2: Radial velocity versus phase (ϕ), using the ephemeris in equation 8.2.

plot between dates HJD 2446319 and HJD 2446369 indicated that the maximum value the period can have is approximately 22 days. Trial velocity modulo orbital phase plots resulted in a period of 21.82 ± 0.01 days giving the only reasonable fit to the data. The ephemeris

$$HJD = 2446317.5 \pm 21.82\ E \qquad (8.3)$$

based on that period has been used to plot the data modulo orbital phase in figure 8.3.

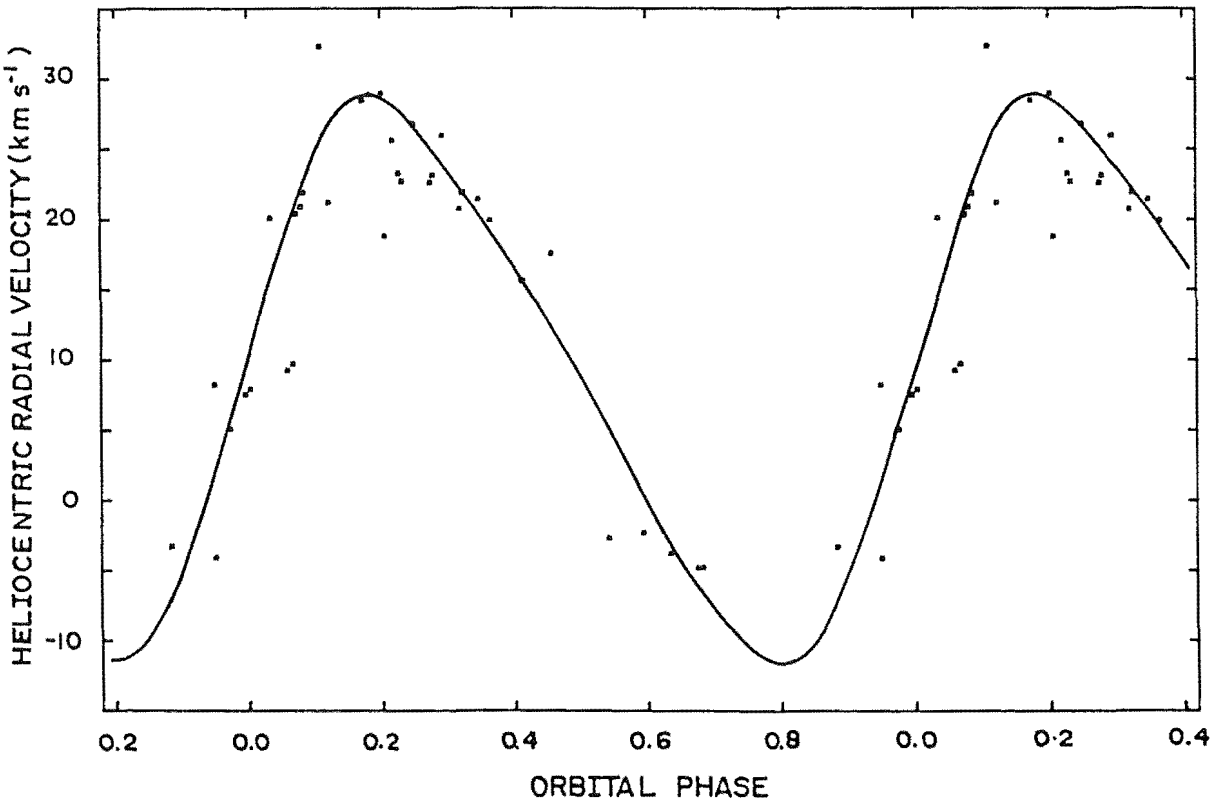


Figure 8.3: As for figure 8.2, except using the new ephemeris given in equation 8.3. The solid line is an eyeball fit to the data.

Five observations in table 8.2 were not used to determine the ephemeris. One did not have a dispersion solution, two had observational difficulty from which flexure was expected, and the observations on HJD 2446537.488 and HJD 2446538.032 had notable spectral peculiarities which will be discussed elsewhere.

8.3.2 Hα Line Profile Variability

An investigation of the temporal dependence of the Hα line profile variations, and the phase dependence of those variations has been carried out. The investigation uses the spectrum of HJD 2446319.839 as its reference point because that spectrum exhibits virtually no Hα emission activity. Regrettably, the unfiltered signal-to-noise ratio of that spectrum was only 40:1 because its primary purpose was to test the instrument. It will hereafter be referred to as the reference spectrum.

Under the assumption that the reference spectrum represents the underlying photospheric absorption spectrum of the star, each spectrum was scaled to its continuum level, translated to its geocentric radial velocity, and then differenced with it. The residual explicitly gives the sum of the chromospheric emission profile and the variations in both the photospheric spectrum and telluric spectrum. The temporal sequence of spectra collected between HJD 2446319.839 and HJD 2446323.876, which starts with the reference spectrum, is given in figure 8.4, with the corresponding residuals shown in figure 8.5. A broad absorption feature displaced by -100 km s^{-1} from the photospheric Hα line is seen to form and then decrease in strength over this period of 4 days, which table 8.3 shows to occur at the peak radial velocity.

To determine if the feature is phase dependent, the same procedure has been applied to the three spectra collected between HJD 2446535.060 and HJD 2446537.119. They are the only other digital spectra at approximately the same phase, and are plotted with their residuals in figure 8.6. While the emission profile is considerably stronger than in the earlier case, an absorption feature can be seen developing with a similir profile but smaller equivalent width than the earlier case. This absorption feature is displaced by -50 km s^{-1} from the photospheric line.

The two image tube plates of Collier (1982) that were exposed at the phases of the reference and peak absorption spectra have been traced on the Joyce-Loebl microdensitometer at the University of Canterbury. They are reproduced in

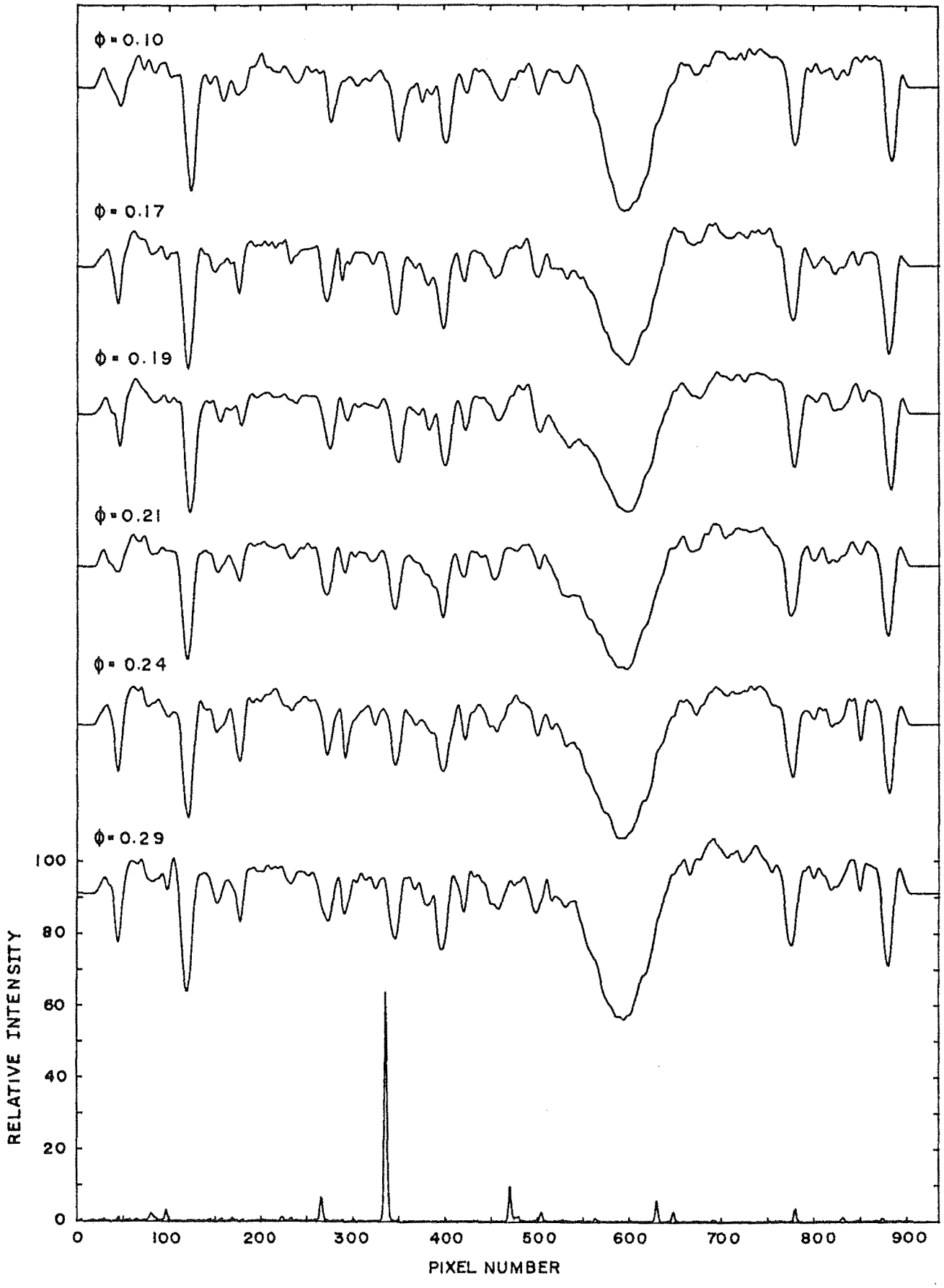


Figure 8.4: Temporal sequence of Hα-region absorption spectra collected at phases according to equation 8.3. The reference spectrum (top) and comparison spectrum (bottom) are shown.

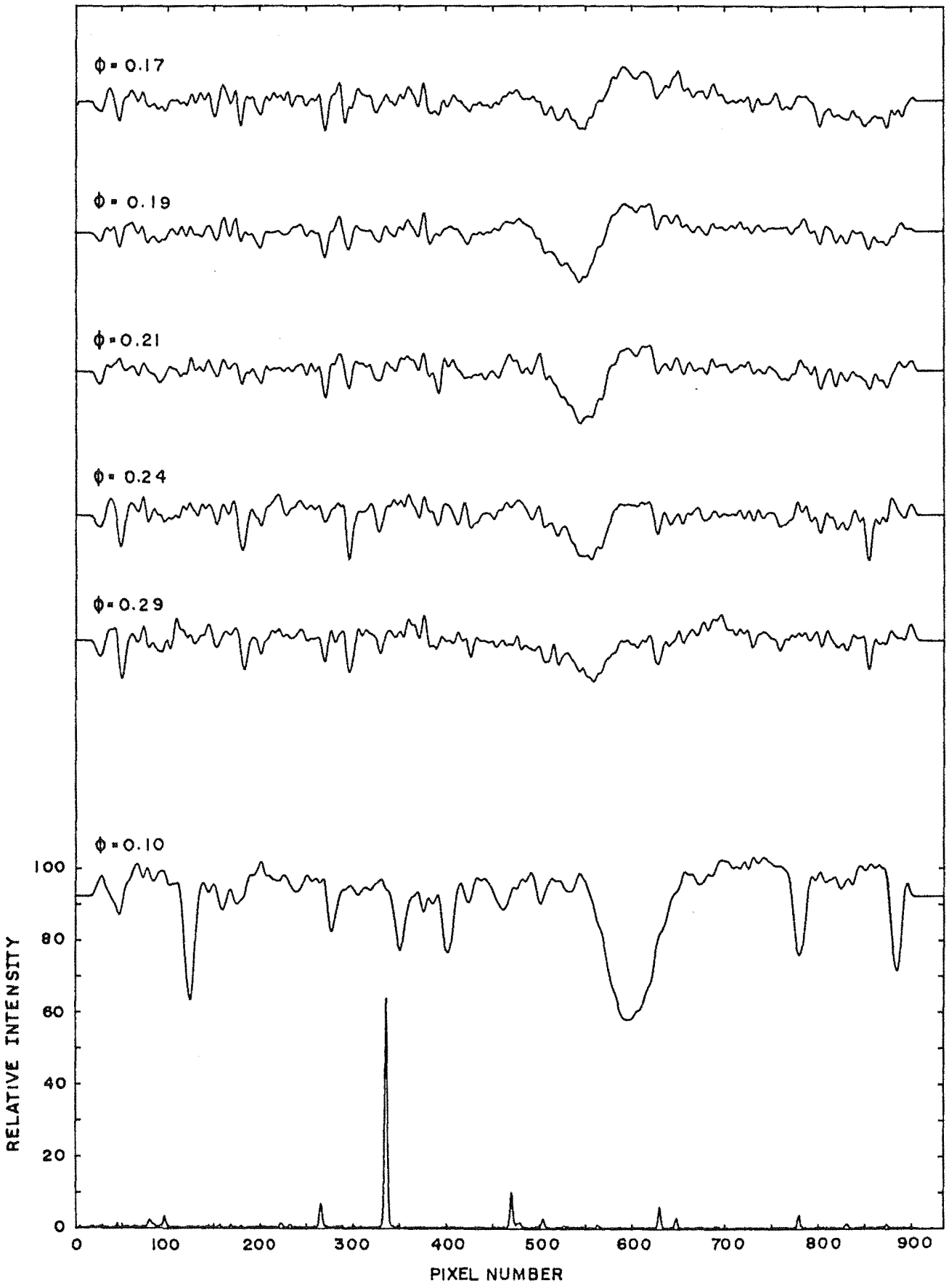


Figure 8.5: Temporal sequence of residual spectra (see text), corresponding to the spectra given in figure 8.4. The reference and comparison spectra are shown at the bottom.

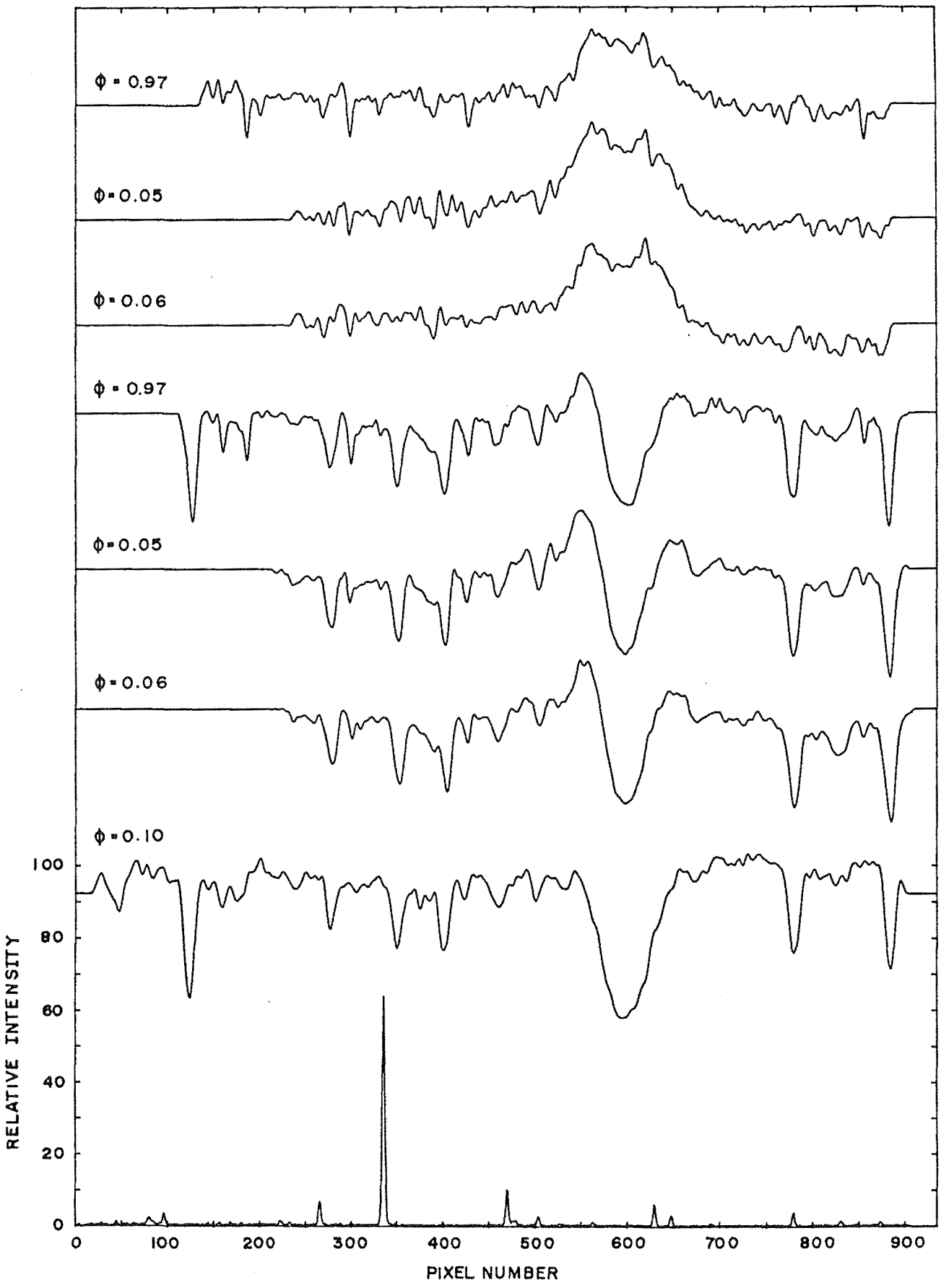


Figure 8.6: Temporal sequence of three residual spectra, and their corresponding spectra, at a similar phase to those shown in figures 8.4 and 8.5.

figure 8.7 with the similar phase digital spectra, and illustrate that the plate spectra have recorded the absorption feature being formed on a similar time scale, but with a smaller amplitude.

The Hα spectra inclusive of HJD 2446346.867 and HJD 2446369.077, form two temporal sequences which are separated by one cycle, and which overlap in phase. Their residuals are given in figure 8.8. The first sequence illustrates, in the absence of the absorption feature, the emission variability that is possible on a short time-scale of about 2 days. The second sequence partially overlaps with the end of the sequence given in figures 8.4 and 8.5. It appears to show the Hα absorption feature decline in strength to zero, which combined with the first two sequences, indicates that the absorption feature exists between approximately phase 0.95 and 0.35. This feature is not seen in any spectra at other phases.

8.3.3 The April 1986 Hα Spectra

The spectrum which was integrated on HJD 2446537.488, supposedly of HR4492, is shown in figure 8.9. It is one of two that were collected on successive days following the sequence given in figure 8.6, for which the observer is confident that the star was correctly identified.

The previously determined radial velocities for these observations are equal to the systemic velocity of HR4492, but the average photon arrival rate during those integrations was approximately a factor of 2½ lower than the.expected rate for HR4492 in the prevailing observing conditions. Therefore given that the spectrum resembles the central section of the Hα profile in an A-type star, a possible explanation is that the active K-giant in HR4492 has been eclipsed in some way, resulting in HD101380, which is about 0.8 magnitudes fainter, dominating the spectrum.

An incident which supports the correct identification of the star occurred on approximately HJD 2446279 when a short duration detector test integration was made on HR4492. The frame was disregarded because a misidentification was assumed

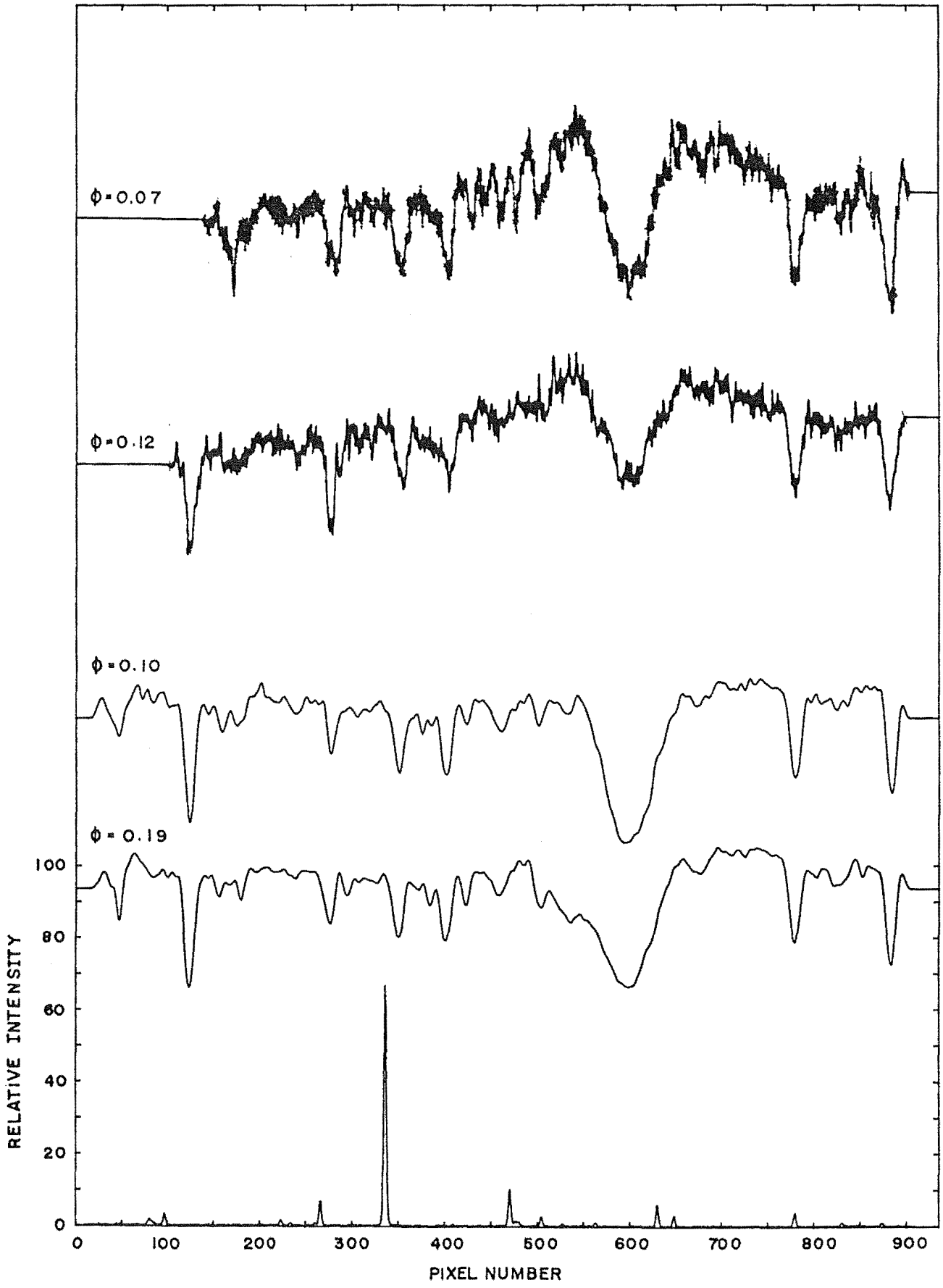


Figure 8.7: Two Hα image tube spectra at similar phases as the digital spectra. The reference spectrum is also shown.

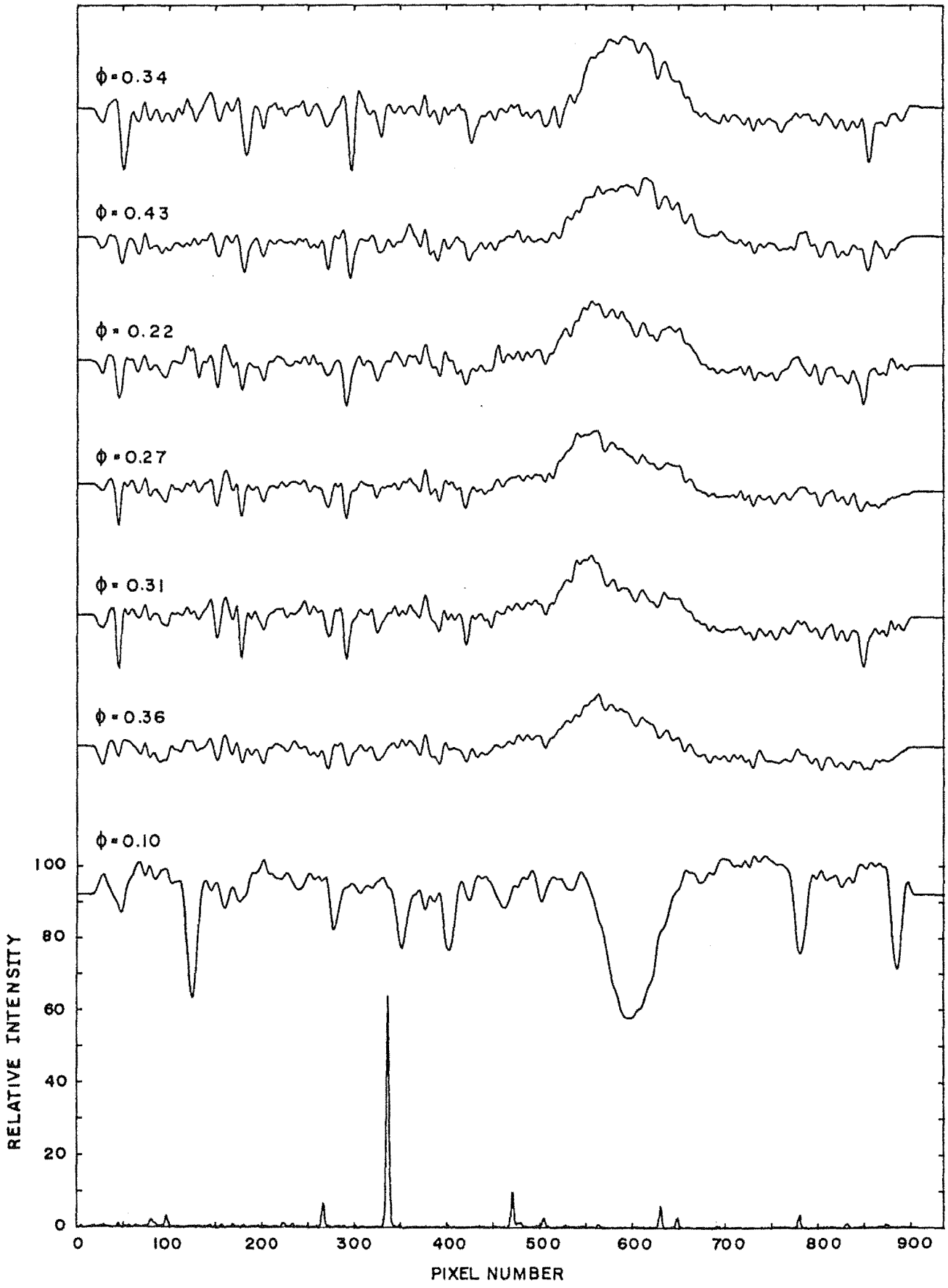


Figure 8.8: Two temporal sequences, at similar phases but on successive cycles, of residual spectra showing the changing Hα emission and absorption line profiles.

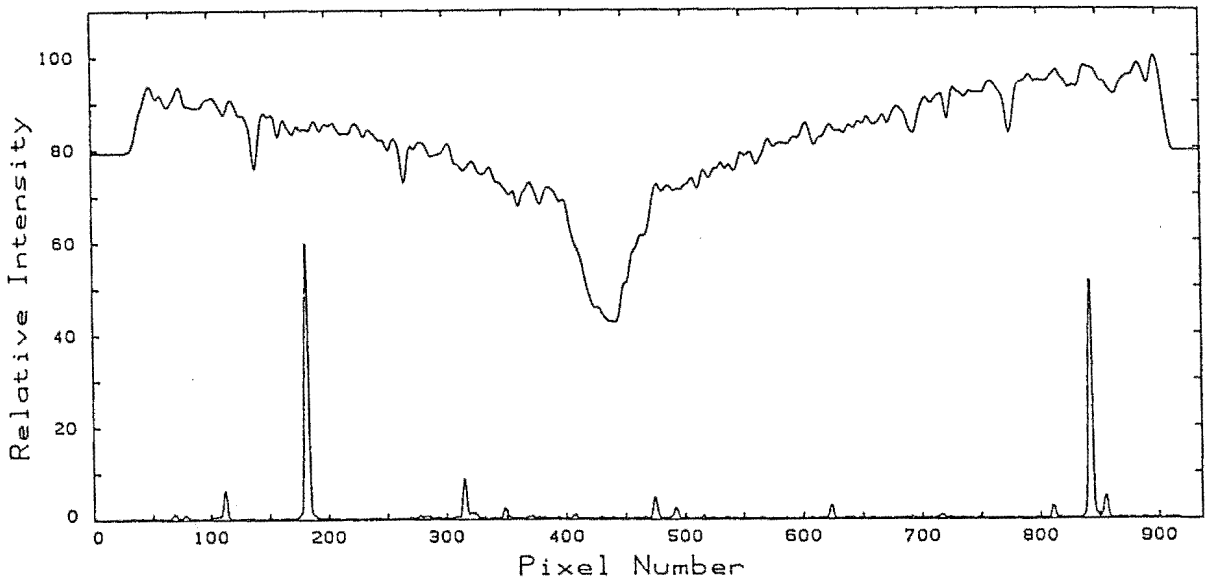


Figure 8.9: Possible Hα spectrum (at ϕ=0.08) of HD101380, the visual companion of HR4492.

when the spectrum had the appearance of an A-star. The 'observations' have approximately the same phase.

8.3.4 Helium and Lithium Observations

Following a suggestion by Lambert (1985), spectra were obtained in the helium D_3 region to determine if that feature was being formed within the chromosphere. A high signal-to-noise ratio spectrum was also integrated in this region for the A7Vn star α Pictoris, which is too cool to exhibit a photospheric D_3 line. Therefore that spectrum will indicate the position of the four telluric lines which are invariably blended with D_3. With the α Pic spectrum for a reference, the three HR4492 D_3 region spectra are shown in figure 8.10, which clearly show the detection of D_3. Collier's Hα region plates also contain the D_3 region, and so have been traced. It is unclear whether or not equivalent width variations seen in D_3 between these plates are solely due to variations in the telluric line strengths, or show a stellar modulation. This was not pursued because the variations were not significantly above the noise level in the plates.

Following the detection of chromospheric D_3, a spectrum

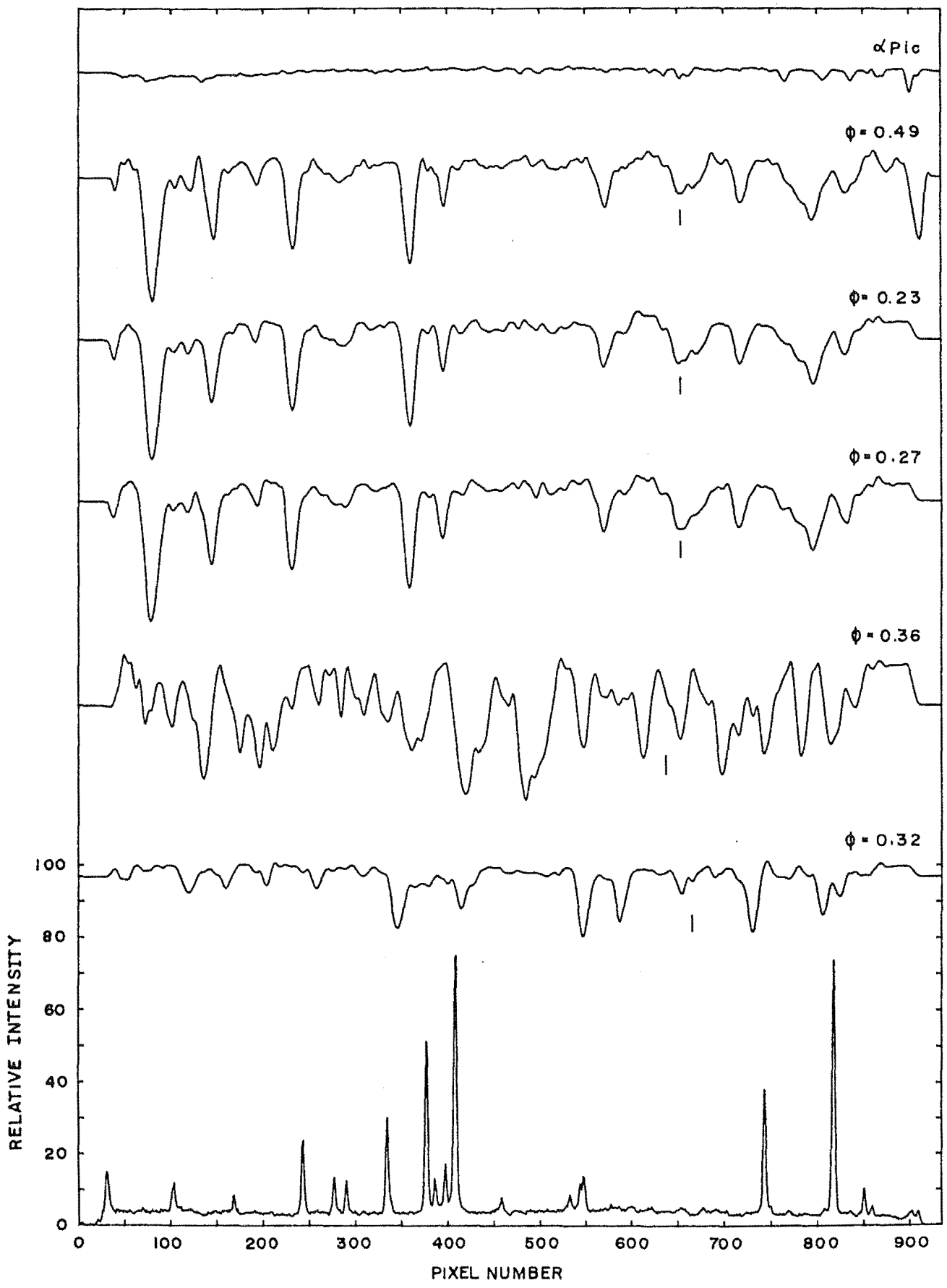


Figure 8.10: A sample of HR4492 spectra showing 3 spectra around λ≈5876Å (D_3), one spectrum around λ≈4686Å (HeII), and one spectrum (with its comparison) around λ≈6707Å (Li I).

of the region centered on the He II 4686 Å line was integrated. That feature is not detected in the spectrum.

A spectrum centered on the Li I 6707 Å region has detected the ^{7}Li 6707.927Å line, as indicated in figure 8.10.

8.4 Discussion

Collier's incorrect determination of the HR4492 ephemeris arose for two reasons. His technique allowed the statistical weight of large groups of observations to significantly outweigh those of the smaller groups, thereby effectively reducing the number of groups which determined the ephemeris to an unacceptable number. Also the poor phase coverage and sparseness of the observations over the interval in which they were collected resulted in considerable aliasing in the solution.

The decrease in the period, by a factor of 2½, moves HR4492 closer to the values in Hall's working definition of the RS CVn class. However Collier (1986) reports that the selection effect that results in Hall's work, where the objects he observes are usually eclipsing variables, has created the unnecessary constraint of requiring the period to be between one day and two weeks.

The three sets of data that fall near the radial velocity maximum in figure 8.3 exhibit different maximum velocities and gradients following maximum velocity. Those gradients appear to increase with increasing maximum velocity, and by examining the corresponding spectra, are seen to also be increasing with decreasing Hα-emission activity. The scatter within the individual groups of data is significantly smaller than the differences shown, which indicates that the radial velocity curve is a function of individual cycle. As a result the curve in that figure represents the average of the data, rather than being a curve for a particular cycle.

The absorption line profile distortions reported by Fekel (1980), which have subsequently been used for Doppler imaging of starspots by Vogt and Penrod (1983), are a possible explanation of the above behaviour. Systematic velocity shifts would be expected which depend upon the distribution

of, and the degree to which spots cover the visible face of the star, and upon the value of $v_e \sin i$. The amplitude of the variation would be expected to depend upon the amplitude of the emission activity because it is directly related to the degree of spot activity. The shift would be expected to vary as the distribution of spots moved onto, across, and off the visible disk of the star. In order to adequately model this behaviour, simultaneous photometry and spectroscopy will be essential to interpret the variations and their dependence upon the photometric spot waves.

The blue shifted Hα absorption feature which appears near peak radial velocity could have been interpreted from figures 8.6 and 8.8 as two emission peaks if it were not for the observations in figure 8.5. The features cyclic behaviour, its phase dependence, and high velocity exclude the possibility of it being the Hα core of HD101380. Collier's (1982) conclusion that the K-star in HR4492 is filling its Roche lobe indicates that mass transfer is the probable cause of the feature. A mass stream of sufficient optical thickness, passing in front of the K-star as we see it, would result in a velocity-shifted absorption feature. It might be expected that the strength of the absorption feature and the emission strength would be anti-correlated because the mass stream would occupy volume in the chromosphere which would normally be contributing to the emission. This trend appears in the observations. In order for a meaningful model to be constructed of such a mass stream, reasonably complete radial velocity curves must first be collected over the duration of the feature and within a number of successive cycles. The model might be similar to that given by Peters (1973) for the B-type star HR2142 which exhibits shell phases.

The April 1986 observations will not warrant much attention until the spectra can be confirmed by future observations of the total system. If confirmation spectra are obtained, it poses a diagnostic dilemma because the HD101380 system is too small to eclipse HR4492, and it would be very difficult to classify the secondary star in HR4492 if it is the secondary which is eclipsing the primary. This is because it must be $\approx 40\ R_\odot$, $\approx 0.8\ M_\odot$, and considerably less luminous than the primary. A possible explanation results from an

accretion disk of the less massive secondary star being larger than that of the primary star. If sufficient mass is accumulated in the accretion disk of the secondary, either before it is either lost from the system or accreted onto the secondary, that confined mass could possibly eclipse the primary star.

CHAPTER NINE

SUMMARY AND FUTURE WORK

9.1 Summary

This thesis has discussed the design and development of a solid-state linear diode array (LDA) image detector system for use with the MJUO échelle spectrograph. Detailed electromechanical design techniques, of significance to astronomical instrumentation, have been presented. Their application has been described by discussing a complete electromechanical design for the detector. This was found to allow each electronic sub-system, implemented within that design, to achieve its theoretical level of performance.

The requirements for the video processing electronics of a solid-state image detector were explicitly developed, and were then used to design the electronics for this detector. Subtle sources of electronic instability, which can appear as noise or base-line shifts, were identified and controlled in this design. In particular, differential non-linearity was identified in an existing preamplifier design, and so an alternative design was implemented.

The readout noise of the entire detector system was measured to be 200 e^-/h pairs for a noiseless signal source of zero impedance to ground. This increased to 350 e^-/h pairs when the impedance of this source was equal to that of the diode array, due to an additional noise contribution of 290 e^-/h pairs. The net readout noise with the RL936F/30 diode array was 450 e^-/h pairs, which is the quadratic sum of the detector system noise with the two 210 e^-/h pair samples of diode capacitance thermodynamic noise. Thus the diode array was not found to contribute any noise in excess of its theoretical thermodynamic noise.

A temperature controller was developed for use with sensors which are cooled in cryogenic dewars. A short term control precision of 1.6 mK r.m.s. was achieved which is due entirely to the theoretical noise of the temperature sensor. The long term precision over all operating conditions was ±20 mK, which is dependent on the design of the dewar.

The hardware and software which provide interactive instrument control and data reduction were described. In particular, they provide flexible control of the detector sub-systems during data acquisition and testing, and enable a high level of data reduction to be undertaken while the detector is integrating.

An observational programme has been carried out with this detector system on the southern RS CVn system HR4492. Radial velocity measurements with a precision of ±0.5 km s^{-1} have enabled a new ephemeris for the binary motion to be determined, namely HJD = 2446317.5 ± 21.82E. It was used to interpret Hα line profile variations in terms of probable mass transfer within the system.

This LDA detector system will mean that future spectroscopic observational programmes at Mount John University Observatory will be able to acquire spectra with significantly higher spectrophotometric accuracy and geometrical stability than has previously been achieved.

9.2 Future Work

In the initial stages of the detector development, the higher numbered half of the diode pairs on the odd shift register exhibited non-Gaussian noise which was considerably in excess of the readout noise. However during the mechanical modifications to the thermal link in February 1986, handling of the preamplifier printed circuit board caused major damage to both shift registers. It is believed that resting this board on a perspex bench top allowed electrostatic discharge damage to occur as a result of static charge entering the then unprotected connectors for the clock lines. The readout noise increased to $\sigma_r \approx 1500$ e^-/h pairs, and approximately 50 diodes developed either bulk or surface traps of typically 100,000 e^-/h pairs depth. Subsequent tests of the video processing electronics with the video line connected both directly, and through a capacitance C_v to ground, found that the noise levels were still 200 and 350 e^-/h pairs respectively. On advice from EG&G Reticon, the diode array was baked at 125 ^oC for 3 days in an attempt to repair the damage. While the

readout noise did not change, 90% of the traps initialy disappeared, only to return with a time constant of approximately 3 days.

As a consequence of the February damage, the planned testing of the system has not been possible. Regretably the data available from before this date, which is suitable for testing, is very sparse because the Data Acquisition System software was still under development. Therefore a number of tests will be given below for establishing the performance of the system when the recently acquired RL1872F/30 diode array is installed. These tests will be combined with some suggested improvements to the system.

9.2.1 Characteristics and Calibration

The accuracy of the technique that was used in section 5.3.1 to determine the system gain, the number of e^-/h pairs per LSB, is unknown. However the system gain can be determined accurately by the noise variance method given by Marcus, Nelson, and Lynds (1979), whose only assumption is that the detector is linear. Therefore this method should be used to accurately calibrate this important system parameter, and to establish the accuracy of the former technique. As a result, the readout noise and rate of thermal leakage will be accurately calibrated.

The above method determines the noise as a function of signal level. Therefore any noise in excess of the theoretical noise, the quadratic sum of the readout and photon shot noise, can be identified as a function of signal level. This ability should be used to search for excess noise at the zero signal level, which could arise from surface and bulk traps. It should also be used near the maximum system signal level to determine if the video processing electronics exhibit a signal level excess noise.

A key design goal of the video processing electronics was to achieve a negligible differential non-linearity error. Differential non-linearity can be detected in quotient frames formed from flat-field frames of different signal levels. It would appear as a residual pattern in the quotient frame, and as enhanced power at its characteristic frequencies in the power spectra of those frames. Therefore a sequence of

flat-field frames should be obtained with different signal levels, and their possible quotient frames and resulting power spectra should be formed and inspected for differential non-linearity.

To ensure the electronic baseline is stable, the diode array must be in thermal equilibrium with the cold block. Therefore the thermal time constant of the diode array package must be determined so that the correct amount of time can elapse between the block coming under temperature control, and the first integration being performed. This time constant can be determined from a sequence of fixed-pattern frames collected between that first time, and the time at which equilibrium is reached. Equilibrium is reached when the fixed-pattern readout frames do not change with time.

9.2.2 Detector Operation

If image lag was detected with the test in section 9.2.1, a special software routine should be written for initializing the array. Instead of using the 600 ns reset pulse width of the readout software, it should use a 249 μs width which starts 1 μs after the diode is accessed, and ends at the same time as the readout reset pulse would have. This length of time is expected to be far more than is necessary to completely reset the array in a single operation.

It is not known if the optimum number of clock edges are received by the array before the start pulse is issued. While an upper limit is placed upon this number by the self-heating of the array, a lower limit also possibly exists in order to ensure that the clock driver electronic devices have reached their equilibrium operating temperatures by the readout time of the first diode pair. A range of different values for this number should be used to determine if the fixed-pattern readout frames exhibit any detectable change. If a change is detected, this same information will determine the optimum value.

Flexible control of the relative clock edge positions, the clock amplitudes, and the bias voltage has been designed into the detector electronics. This control should be used to determine the operating values for those parameters which give the minimum readout noise.

9.2.3 Data Reductions

One subtle but significant problem exists with the flat-field division and baseline subtraction software routines. It arises because the flat-field division must be performed before the baseline is removed, and because the general shape of the flat-field with an échelle spectrograph is that of the underlying spectral order profile. It follows that the component of the quotient frame which corresponds to the baseline will have the shape of the flat-field frame. Therefore the normal linear interpolation of the baseline across the array will leave the curvature component of the baseline in the quotient frame, which will distort the shape of the stellar continuum. This error can become significantly larger than the readout noise when the order curvature is high, and for the typical baselines of longer integration times. Thus the baseline subtraction routine must be rewritten so as to interpolate the baseline across the array using the curvature and end-points of the flat-field frame.

To further facilitate the accurate subtraction of the baseline, very long integrations on the baseline should be obtained at the standard operating temperatures of the array. These should be scaled by the software as determined by the masked pixel levels and the flat-field shape, and used for subtracting the actual baseline. In obtaining the baseline integrations, fixed-pattern frames from before and after the baseline frame should be compared to ensure that the electronic baseline shift is negligible. Also, a number of baseline frames should be obtained for a given temperature so that cosmic ray events can be identified, and a single frame formed which does not have any such events.

ACKNOWLEDGEMENTS

During the course of my thesis I have been fortunate to have had mixtures of guidance, support, and assistance from a great number of people. This has been of considerable significance to me, and I wish to express my gratitude to those people.

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Dr Colin Hooker shared his wealth of experience in cryogenic matters with me, and pointed me in the direction which lead to the temperature controller.

Almost endless componentry was ordered at short notice by Derek Lipyeat. His uncomplaining efficienty at dealing with unusual requests and changes of mind has been a great help. In all my dealings with the other office staff they have been most friendly and efficient.

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Professor David Lambert showed great balance as he pointed a 1000 W photo-flood at the dome from atop a ladder during the first flat-field integrations. Martin Begley obtained the April and May integrations of HR4492, including the unusal ones which have caused much discussion.

Graeme Kershaw designed the very successful rotational mechanism for the dewar lid. Bruce Bradshaw did the metal work for the interface chassis with Stephen Hemmingsen. As well, Stephen did a great many unusual odd jobs for me.

Many high vacuums were made in the dewar by Tom Walker who, with Ron Culley, kept the liquid nitrogen flowing.

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Much of my first year was spent in the Department of Electrical and Electronic Engineering workshop. Dr Bob Hodgson arranged for my presence during that year, and pointed me to Senturia and Wedlock (1975) for my first contact with electronics. Many of my design techniques have been sparked from this book. I am grateful to Mike Houstead for 'mothering' me as I learnt the like of soldering, and as I gained valuable experience with Duncan Hall's linear diode array development system. Mike La Hood pointed out to me that the design of the circuitry is only part of the total design of a system. Richard Cox asked me many questions about practical physical problems, which I unsatisfactorily answered.

Dr Noel Doughty and Dr Geoff Stedman installed me on T^3 for preparing this thesis. Mrs van der Borch very ably traced virtually every figure, and I am most grateful for the results she achieved. Warrick Lawson helped out when time was short by preparing the photographs for mounting.

My dealings with the Engineering Library have always ben most pleasurable. They set a fine example of how a library can really work for the user.

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I wish to thank my parents for the care and understanding they gave to my education, and to my interest in astronomy. I still remember the night Dad showed me the Southern Cross when I was a small boy.

Finally, I express my sincerest thanks to my wife Lyndy, who has endured much, been most patient, and has given so much support over these years.

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APPENDIX ONE

OPERATIONAL AMPLIFIERS

As operational amplifiers are the basic building block of the analogue circuitry in this work, their basic operating principles must be understood to enable that circuitry to be considered. Also, several general results are required for use in calculating parameters when applying the amplifiers.

There are three operational amplifier terminals used by the signal conditioning circuitry of the amplifier. They are the input non-inverting, I+, and inverting, I-, terminals, and the output terminal. The properties of an ideal operational amplifier include the following:

1) The input impedance of I+ and I- is infinite, therefore no current passes through those terminals regardless of their input voltages.

2) The output voltage remains constant when the voltage difference between the input terminals, the differential input voltage, is zero.

3) The amplification of the voltage difference between the input terminals is infinite, that is, the differential input voltage is infinite.

4) The output impedance is zero.

Property #3 above requires the different input voltage to be zero if an output voltage other than $\pm\infty$ is to be obtained. Thus negative feedback, the application of the output signal in some conditioned form to the inverting terminal, is always used to stabilize this intrinsically unstable behaviour. Therefore consider figure A1.1 which shows an amplifier with a feedback resistor, R_f, providing negative feedback, and an input resistor, R_i. When the

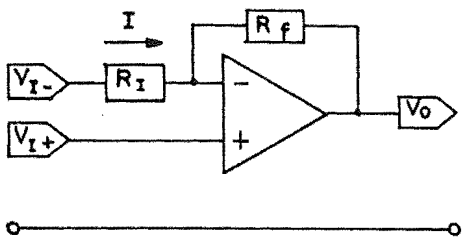

Figure A1.1: An operational amplifier with negative feedback.

circuit has stabilized after the application of the input voltages, V_{i+} and V_{i-}, the voltage at the inverting terminal must be equal to V_{i+}. It follows that the input current must be

$$I = \frac{(V_{i-} - V_{i+})}{R_i} \quad . \tag{A1.1}$$

Because I- has an infinite input impedance, from #1 above, this current must then pass through the feedback resistor and in doing so, develop a potential difference between its input and output sides of

$$V_{i+} - V_o = IR_f \quad . \tag{A1.2}$$

Therefore substituting equation A1.1 into equation A1.2 gives

$$V_{i+} - V_o = \frac{R_f}{R_i} (V_{i-} - V_{i+}) \quad , \tag{A1.3}$$

which can be rearranged to give the output voltage in terms of the input voltages, the transfer function, as

$$V_o = \left[1 + \frac{R_f}{R_i}\right] V_{i+} - \left[\frac{R_f}{R_i}\right] V_{i-} \quad . \tag{A1.4}$$

The behaviour of the two most common applications of this feedback network can be found from equation A1.4.

In the first application, the input side of the input resistor is connected to ground as shown in figure A1.2a, and so $V_{i-} = 0$ volts. This configuration is called a non-inverting amplifier, and its transfer function follows

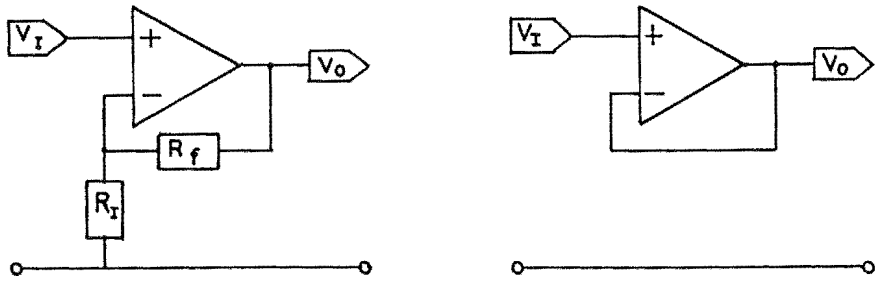

Figure A1.2: Two examples of non-inverting amplifiers.

from equation A1.4 as

$$V_o = GV_i \quad ; \quad G = \left[1 + \frac{R_f}{R_i}\right] \quad , \tag{A1.5}$$

where G is the gain of the amplifier. In the limit of R_f

going to zero, and R_i going to infinity, the circuit becomes that of figure A1.2b. This configuration has unity gain, and is sometimes referred to as a buffer because of its infinite input impedance.

In the second application of the feedback network (figure A1.2), the I+ terminal is connected to ground to give $V_{i+} = 0$ volts and the configuration is shown in figure A1.3.

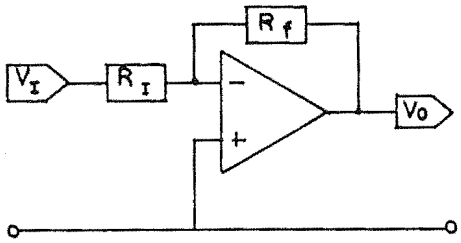

Figure A1.3: An inverting amplifier.

This configuration is called an inverting amplifier, and has a transfer function determined from equation A1.4 of

$$V_o = GV_i \quad ; \quad G = \left[- \frac{R_f}{R_i} \right] \quad , \qquad \text{(A1.6)}$$

where G is the gain of the amplifier.

While the feedback components in figure A1.1 are resistors, they could equally have been networks of passive components with net reactances of Z_f and Z_i. It follows that in this general case, the transfer function is

$$V_o = \left[1 + \frac{Z_f}{Z_i} \right] V_{i+} - \left[\frac{Z_f}{Z_i} \right] V_{i-} \quad . \qquad \text{(A1.7)}$$

APPENDIX TWO

THERMAL NOISE [1]

Thermal noise is caused by the random thermally excited vibration of the charge carriers in a conductor. This carrier motion is similar to the Brownian motion of particles. From studies of Brownian motion, thermal noise was predicted. It was first observed by J.B.Johnson of Bell Telephone Laboratories in 1927, and a theoretical analysis was provided by H. Nyquist in 1928. Because of their work thermal noise is called Johnson noise or Nyquist noise.

In every conductor at a temperature above absolute zero the electrons are in random motion, and this vibration is dependent on temperature. Since each electron caries a charge of 1.59×10^{-19} C, there are many little current surges as electrons randomly move about in the material. Although the average current in the conductor resulting from these movements is zero, instantaneously there is current fluctuation that gives rise to a voltage across the terminals of the conductor.

The *available noise power*, N_t, in a conductor is found to be proportional to the absolute temperature and to the bandwidth of the measuring system. In equation form this is

$$N_t = kT\Delta f \qquad \text{(A2.1)}$$

where k = Boltzmann's constant = 1.38×10^{-23} W s K^{-1} ,

T = temperature of the conductor in degrees Kelvin,

and Δf = *noise bandwidth* of the measuring system in hertz.

At room temperature (290 K), for a 1-Hz bandwidth, evaluation of equation A2.1 gives $N_t = 4 \times 10^{-21}$ W. This is - 204 dB with reference to 1 W.

The noise power predicted by equation A2.1 is that caused by thermal agitation of the carriers. Other noise mechanisms can exist in a conductor, but they are excluded from consideration here. Thus the thermal noise represents a minimum level of noise in a resistive element.

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[1] from Motchenbacher and Fitchen (1973), pp. 9-16.

In equation A2.1 the noise power is proportional to the bandwidth. There is equal noise power in each hertz of bandwidth; the power in the band from 1 to 2 Hz is equal to that from 1000 to 1001 Hz. This results in thermal noise being called 'white noise'. White implies that the noise is made up of many frequency components just as white light is made up of many colours. A Fourier analysis gives a flat plot of noise versus frequency. The comparison to white light is not exact, for white light consists of equal energy per wavelength, not per hertz.

Thermal noise ultimately limits the resolution of any measurement system. Even if an amplifier could be built perfectly noise-free, the resistance of the signal source would still contribute noise.

Equation A2.1 can be changed into a much more useful form. *Available power is the power than can be supplied by a source when it is feeding a resistance load equal to its internal resistance.* Since available power can be expressed as $E^2/4R$, equation A2.1 can be rewritten as

$$N_t = kT\Delta f = \frac{E_t^2}{4R} . \qquad (A2.2)$$

Therefore the *rms noise voltage*, E_t, of a resistance R is

$$E_t = \sqrt{4kTR\Delta f} , \qquad (A2.3a)$$

where R = real part of the conductor's impedance,
and $4kT = 1.61 \times 10^{-20}$ at room temperature (290 K).

When working with noise voltages it is often necessary to use mean square values of quantities. A symbol commonly used for the mean square value of thermal noise is e_t^2. The overbar represents a mean or average value. Rms is simply the square root of a mean square value, therefore $E_t = \sqrt{(\overline{e_t^2})}$. *Since they are equivalent, both* $\overline{e^2}$ and E^2 *can be used to represent mean square.* An alternative expression for thermal noise voltage is

$$E_t^2 \text{ or } \overline{e_t^2} = 4kTR\Delta f \qquad (A2.3b)$$

Equation A2.3 is very important in noise work. It provides the limit that must be kept in mind. We shall see

that the measure of an amplifier's performance, noise figure, is only a measure of the noise the amplifier adds to the thermal noise of the source resistance. A more complete expression for the thermal noise is given by Motchenbacher and Fitchen (1973).

Several important observations can be made from equation A2.3. Noise voltage is proportional to the square root of bandwidth, no matter where the frequency band is centred. *Reactive components do not generate thermal noise.* The resistance used in the equation is not simply the dc resistance of the device or component, but is more exactly defined as the real part of the complex impedance. In the case of an inductance, it may include eddy current losses. In the case of a capacitor, it can be caused by dielectric losses. It is obvious that cooling a conductor decreases its thermal noise.

As an example we can determine the rms noise voltage of a 1000 Ω resistor with an amplifier noise bandwidth of 1 Hz to be 4 nV. This is a good number to memorize as a benchmark. From this we can scale up or down by the square root of resistance or bandwidth.

The effect of broadband thermal noise must be minimized. Equation A1.3 implies that there are several practical ways. The sensor resistance must be kept as low as possible, and additional series resistance elements must be avoided. Also, it is desirable to keep bandwidth as narrow as possible, while maintaining the bandwidth necessary to pass the signal signature. When designing a system, frequency limiting can be incorporated in one of the later stages.

Even though we have shown that there is a time-varying current and available power in every conductor, this is not a new power source! You cannot put a diode in series with a noisy resistor and use it to power a transistor radio. If the conductor were connected to a load (another conductor), the noise power of each would merely be transferred to the other. If a resistor at 300 K, room temperature, were connected in parallel with a resistor at 0 K, there would indeed be a power transfer from the higher temperature resistor to the lower. The warmer resistor would try to cool down and the other would try to warm up until they came into thermal equilibrium. At

that point there would be no further power transfer.

Thermal noise has been extensively studied. Expressions are available for predicting the number of maxima per second present in thermal noise, and also the number of zero crossings expected per second in the noise waveform. These quantities are dependent on the width of the passband. Formulas are given in Motchenbacher and Fitchen (1973).

NOISE BANDWIDTH

When bandwidth is not the same as the commonly used 3-dB bandwidth. There is one definition of bandwidth for signal and another for noise.

The bandwidth of an amplifier or a tuned circuit is classically defined as the frequency span between half-power points. The half-power points are values on the frequency axis where the signal transmission has been reduced by 3 dB from the central or midrange reference value. A 3-dB reduction represents a loss of 50% in power level and corresponds to a voltage level equal to 70.7% of the voltage at the centre frequency reference.

The noise bandwidth, Δf, is the frequency span of a rectangularly shaped power gain curve equal in area to the area of the actual power gain versus frequency curve. Noise bandwidth is the area under the power curve, the integral of power gain versus frequency, divided by the peak amplitude of the curve. This can be stated in equation form :

$$\Delta f = \frac{1}{G_o} \int_o^\infty G(f_o)\, df \qquad \text{(A2.4)}$$

where Δf = noise bandwidth in hertz,

$G(f)$ = power gain as a function of frequency,

and G_o = peak power gain.

Since power gain is proportional to the network voltage gain squared, the equivalent noise bandwidth can also be written as

$$\Delta f = \frac{1}{A_{vo}^{\,2}} \int_o^\infty [A_v^{\,2}(f)]df \ , \qquad \text{(A2.5)}$$

where $A_v(f)$ = voltage gain as a function of frequency,

and A_{vo} = midband voltage gain.

The equation is more useful in the second form.

The term spectral density is used to describe the noise content in a unit of bandwidth. We know that noise consists of many frequency components; to indicate how these components are distributed if we could plot mean square noise per unit bandwidth against frequency. For a thermal noise source the spectral density S(f) is

$$S(f) = \frac{E_t^2}{\Delta f} = 4kTR \quad V^2\ Hz^{-1} \ . \qquad (A2.6)$$

It is characteristic of white noise sources that the plot of S(f) versus f be simply a horizontal line.

When measuring noise we often work with the rms value of a noise quantity. Thus we might obtain a kind of spectral density by dividing the rms value of a noise voltage by the square root of the noise bandwidth, and obtain

$$\frac{E}{\sqrt{\Delta f}} \quad \text{in units of } V/\sqrt{Hz}$$

The result of this mathematical operation can be interpreted as simply the rms noise voltage in 1 Hz of bandwidth. Note that $E/\sqrt{\Delta f}$ is a symbol for a quantity that can be measured; the units are $V/\sqrt{Hz}$. Often this density function is symbolized by $E/\sqrt{\sim}$, or in the case of a current, $I/\sqrt{\sim}$. Since a bandwidth of 1 Hz is almost always used, the units for these functions are referred to as 'volts per hertz' and 'amps per hertz'.

THERMAL NOISE EQUIVALENT CIRCUITS

In order to perform a noise analysis of an electronic system, every element that generates thermal noise is represented by an equivalent circuit composed of a noise voltage generator in series with a noiseless resistance. Suppose, then, that we have a noisy resistance R connected between terminals *a* and *b*. For analysis, we substitute the equivalent shown in figure A2.1a, a noiseless resistance of the same ohmic value, and a series noise generator with rms value E_t equal to $\sqrt{(4kTR\ \Delta f)}$. This generator is supplying the circuit with multi-frequency noise; it is specified by the rms value of its total output.

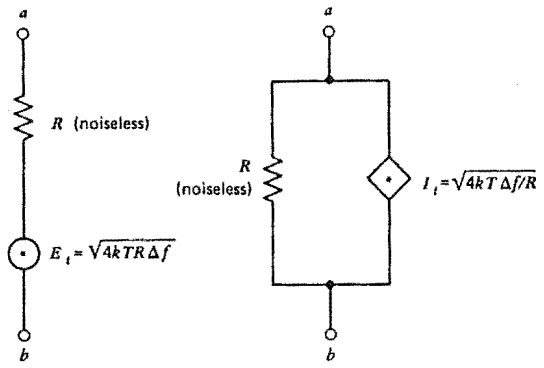

Figure A2.1: Equivalent circuits for thermal noise.

According to Norton's theorem, the series arrangement shown in figure A2.1a can be replaced by an equivalent constant-current generator in parallel with a resistance. The noise current generator I_t will have an rms value equal to E/R, or in this instance

$$I_t = \sqrt{\frac{4kT\Delta f}{R}} \quad . \tag{A2.7}$$

If a voltmeter with infinite input impedance and zero self-noise were connected between *a* and *b*, the thermal noise voltage could be measured. However, because real voltmeters also contribute noise, such a direct reading is not accurate.

The system of symbols that we employ in noise analysis uses the letters E and I to represent noise quantities. *The letter V is reserved for signal voltage.* Because noise generators do not have an instantaneous phase characteristic as is attributed to sine waves in the phasor method of representation, no specific polarity indication is included in the noise source symbols in figure A2.1. Polarity of noise sources is discussed in Motchenbacher and Fitchen (1973).

APPENDIX THREE

LOW-FREQUENCY NOISE [1]

Low-frequency or 1/f noise has several unique properties. If it were not such a problem it would be very interesting. The spectral density of this noise increases without limit as frequency decreases. Firle and Winston (1955) have measured 1/f noise as low as 6×10^{-5} Hz. This frequency is but a few cycles per day.

When first observed in vacuum tubes, this noise was called "flicker effect," probably because of the flickering observed in the plate current. Many different names are used, some of them uncomplimentary. In the literature, names like excess noise, pink noise, semiconductor noise, low-frequency noise, and contact noise will be seen. These all refer to the same thing. The term "red noise" is applied to a noise power spectrum that varies as $1/f^2$.

The noise power typically follows a $1/f^{\alpha}$ characteristic with α usually unity, but α has been observed to take on values from 0.8 to 1.3 in various devices. The major cause of 1/f noise in semiconductor devices is traceable to properties of the surface of the material. The generation and recombination of carriers in surface energy states and the density of surface states are important factors. Improved surface treatment in manufacturing has decreased 1/f noise, but even the interface between silicon surfaces and grown oxide passivation are centres of noise generation.

As pointed out by Halford (1968), 1/f noise is quite common. Not only is it observed in tubes, transistors, diodes, and resistors, but it is also present in thermistors, carbon microphones, thin films, and light sources. The fluctuations of a membrane potential in a biological system have been reported to have flicker noise. No electronic amplifier has been found to be free of flicker noise at lowest frequencies. Halford points out that $\alpha = 1$ is the most common value, but there are other mechanisms with different alphas.

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[1] from Motchenbacher and Fitchen (1973), pp. 19-20.

For example, fluctuations of the frequency of rotation of the earth have an α of 2 and the power spectral density of galactic radiation noise has $\alpha = 2.7$.

Since 1/f noise power is inversely proportional (K_1) to frequency, it is possible to determine the noise content in a band by integration of $K_1 f^{-1}$ over the range of frequencies in which our interest lies. The result is :

$$N_f = K_1 \log_e \left[\frac{f_h}{f_i}\right] . \qquad (A3.1)$$

Symbols f_h and f_i are the upper and lower frequency limits of the band being considered.

The mean square value of the corresponding noise voltage is

$$E_f^2 = K\log_e\left[\frac{f_h}{f_i}\right] = K\log_e\left[1 + \frac{\Delta f}{f_i}\right] \simeq K\frac{\Delta f}{f} . \qquad (A3.2)$$

When the band is 1-Hz wide, $f_h = f_i + 1$. Then equation A3.2 can be written

$$S(f) = \frac{K}{f} \ V^2 \ Hz^{-1} , \qquad (A3.3)$$

which is the spectral density of 1/f noise.

Because 1/f noise power continues to increase as the frequency is decreased, we might ask the question, why is the noise not infinite at dc? Although the noise voltage in a 1-Hz band may theoretically be infinite at dc or 0 frequency, there are practical considerations that keep the total noise manageable for most applications. The noise power per decade of bandwidth is constant, but a decade such as that from 0.1 to 1 Hz is narrower than the decade from 1 to 10 Hz. But, when considering the 1/f noise in a dc amplifier, there is a lower limit to the frequency response set by the length of time the amplifier has been turned on. This low-frequency cutoff attenuates components with periods longer than the "on" time of the equipment.

A numerical example may be of assistance. Consider a dc amplifier with upper cutoff frequency of 1000 Hz. It has been on for 1 day. Since 1 cycle/day corresponds to about 10^{-5} Hz, its bandwidth can be stated as 8 decades. If it is on for 100 days we may add 2 more decades or $\sqrt{2}$ times its 1-day noise. The noise per hertz approaches infinity, but the

total noise does not.

A fact to remember concerning a 1/f noise-limited dc amplifier is that measurement accuracy cannot be improved by increasing the length of measuring time. In contrast, when measuring white noise, the accuracy increases as the square root of the measuring time.

Firle, J.E., and Winston, H.: 1955, *Bull. Am. Phys. Soc.*, 30, 2.

Halford, D.: 1968, "A General Model for f^{α} Spectral Density Random Noise with Special Reference to Flicker Noise 1/f," Proc. IEEE, 56 #3 , 251.

APPENDIX FOUR

ADDITION OF NOISE VOLTAGES [1]

When sinusoidal signal voltage sources of the *same frequency and amplitude* are connected in series, the resultant voltage has twice the common amplitude if they are in phase, and combined they can deliver four times the power of one source. If, on the other hand, they differ in phase by 180^{o}, the net voltage and power from the pair is zero. For other phase conditions they may be combined using the familiar rules of phasor algebra.

If two sinusoidal signal voltage sources of *diffrerent frequencies* with rms amplitudes V_1 and V_2 are connected in series, the resultant voltage has rms amplitude equal to $\sqrt{(V_1^2 + V_2^2)}$. The mean square value of the resultant wave, V_r^2, is the sum of the mean square values of the components ($V_r^2 = V_1^2 + V_2^2$).

Equivalent noise generators represent a very large number of component frequencies with a random distribution of amplitudes and phases. When independent noise generators are series connected, the separate sources neither help nor hinder one another. *The output power is the sum of the separate output powers, and consequently it is valid to combine such sources so that the resultant mean square voltage is the sum of the mean square voltages of the individual generators.* This statement can be extended to noise-current sources in parallel.

The generators E_1 and E_2 shown in figure A4.1 represent uncorrelated noise sources. We form the sum of these voltages

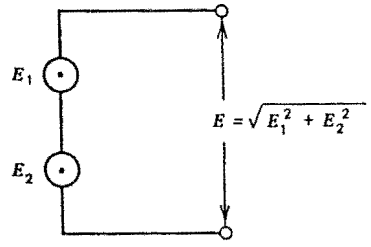

Figure A4.1: Addition of uncorrelated noise voltages.

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[1] from Motchenbacher and Fitchen (1973), pp. 16-17.

by adding mean square values. Thus the means square of the sum, E^2, is given by

$$E^2 = E_1^2 + E_2^2 \quad . \qquad (A4.1)$$

Taking the square root of a quantity such as E^2 represents rms. It is not valid to sum the rms voltages of series noise sources. However, one can often neglect the smaller of the two noise signals when their rms values are in a 10:1 ratio. The smaller signal only adds 1% to the overall voltage. A 3:1 ratio has only a 10% effect on the total.

If two resistors are connected in parallel, the total thermal noise voltage is that of the equivalent resistance. Similarly, with two resistors in series, the total noise voltage is determined by the arithmetic sum of the resistances.

APPENDIX FIVE

TEMPERATURE COEFFICIENT RESULTS

A number of temperature dependent components and parameters are used in combinations within this work, for which the net temperature coefficent must be calculated. The definition for the temperature coefficient, TC, of the general quantity Q is

$$TC(Q) = \frac{1}{Q}\,\frac{dQ}{dT} \quad , \qquad (A5.1)$$

where T is the ambient temperature. It has been used to determine the following results.

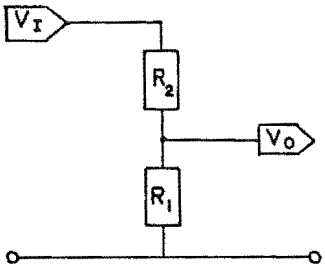


Figure A5.1: A resistor divider network.

The resistor divider network shown in figure A5.1 divides the input voltage, V_{in}, down to the output voltage, V_{out}, as described by

$$V_{out} = A\,V_{in} \quad ; \quad \text{where} \quad A = \frac{R_1}{R_1+R_2} \quad . \qquad (A5.2)$$

The temperature coefficient of the output is

$$TC(V_{out}) = TC(V_{in}) + TC(A) \quad , \qquad (A5.3)$$

where $TC(V_{in})$ is the temperature coefficients of V_{in}, and the temperature coefficient of A is

$$TC(A) = (1-A)\left[TC(R_1)-TC(R_2)\right] \quad . \qquad (A5.4)$$

Often R_1 and/or R_2 will in turn be a combination of resistors, and so the temperature coefficients of the combinations must first be found using the following results.

The temperature coefficient of the net resistance of two resistors, R_1 and R_2, which are used in series is

$$TC(R_1+R_2) = TC(R_1) + TC(R_2) \quad , \qquad (A5.5)$$

and when used in parallel is

$$TC(R_1//R_2) = \frac{R_1}{R_1+R_2}TC(R_2) + \frac{R_2}{R_1+R_2}TC(R_1) \quad . \qquad (A5.6)$$

The gain of a non-inverting amplifier is

$$G = 1 + \frac{R_f}{R_s} \quad , \qquad (A5.7)$$

where R_f and R_s are respectively the feedback and source resistances, whose temperature coefficients result in a temperature coefficient for the gain of

$$TC(G) = \frac{R_f}{R_s+R_f}\left[TC(R_f)-TC(R_s)\right] \quad . \qquad (A5.8)$$

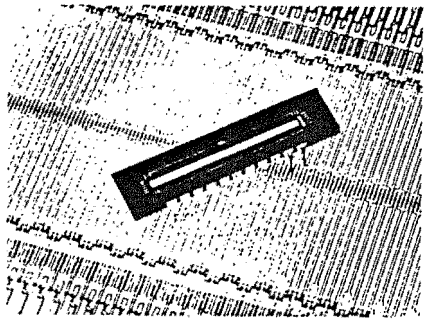
As with the divider network, the resistors may be combinations for which the temperature coefficents must first be calculated.

Finally, when two amplifiers are used in series, the temperature coefficient of their net gain is

$$TC(G_1G_2) = TC(G_1) + TC(G_2) \quad . \qquad (A5.9)$$

RETICON®

RL-1872F AND RL-936F
SOLID STATE LINE SCANNERS



The RETICON RL-1872F represents a major breakthrough in solid state image sensor technology. This self-scanning linear array of 1872 silicon photodiodes is designed primarily for page reader and facsimile applications. For the first time it makes possible high resolution facsimile with a single solid state detector device. The RL-936F is identical in design but is only 936 diodes long. Both devices are fabricated using the most modern silicon-gate MOS technology. Key features include:

- **High resolution—1872 or 936 elements on 15 micron (0.59 mil) centers**
- **On-chip scanning for serial video output**
- **Low power shift register scanning circuit—4 mwatts dissipation**
- **Four parallel video output lines for high data rates—up to 20 MHz**
- **Charge storage mode operation for high sensitivity**
- **Standard dual-in-line package with fused quartz window**

GENERAL DESCRIPTION

The RL-1872F is a monolithic silicon photodiode array containing a row of 1872 photodiodes on 15 micron (0.59 mil) centers. Each diode has an associated capacitance on which photocurrent is integrated until it is read out periodically through a multiplex switch onto one of four video output lines.

Read out is accomplished by a shift register scanning circuit which is driven by four phase clocks. Each scan is initiated by entering a start pulse into the shift register. After initiation of a scan two adjacent diodes are read out simultaneously on each clock transition. A new scan may be initiated immediately after the last pair of diodes has been read out or a longer interval between start pulses may be used to increase the integration time. The devices may be operated at clock rates up to 10 MHz corresponding to data rates up to 20 MHz.

Speed can be traded for sensitivity since the lower the line rate the longer the diodes can integrate photocurrent.

The RL-1872F is supplied in a 22 pin package 0.4 inches wide x 1.6 inches long. The RL-936F is supplied in an 18 pin package 0.3 inches wide x 0.9 inches long. Both packages are black ceramic with a ground and polished quartz window. Both fit into standard integrated circuit sockets. Block diagrams and pin configurations are shown in Figures 1 and 2.

DRIVER REQUIREMENTS

A nominal +5 volt supply is required for the RL-1872F and the RL-936F. The four clock phases and the start pulse should then swing negative by ~11 to ~15 volts with respect to the positive supply. The start pulse should be wide enough to include one positive going transition of ϕ_1 and one positive going transition of ϕ_1'.

A TTL clock and start circuit capable of generating the basic timing is shown in Figure 3. The clock may be supplied externally or generated internally. In the internal mode the clock frequency is set by the 50K ohm potentiometer and the capacitor C_1. A periodic start pulse is generated by counting clock pulses. The count between start pulses is set by grounding various terminals of the 9316 counters. There should be a minimum of 940 clock pulses between start pulses for the RL-1872F and a minimum of 472 for the RL-936F.

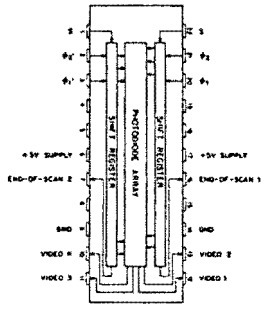


Figure 1. Block Diagram and Pin Configuration of RL1872F.

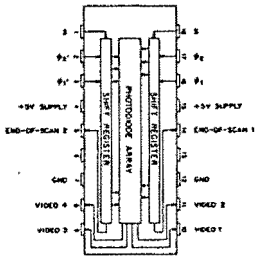


Figure 2. Block Diagram and Pin Configuration of RL936F.

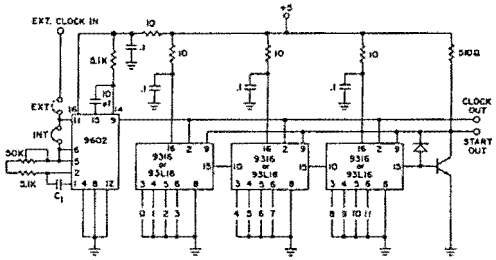


Figure 3. TTL Clock and Counter Circuit for Generating Clock and Start Timing Pulses.

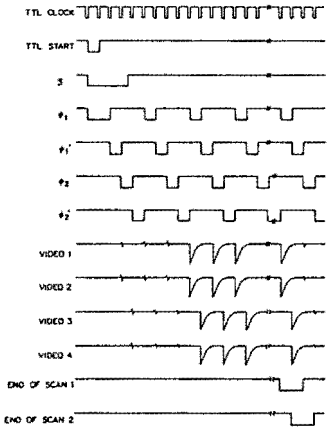


Figure 5. Timing Diagram Showing Clock and Start Inputs and Video and End-of-Scan Outputs.

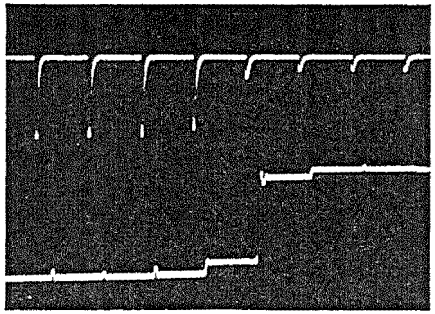


Figure 7. Video Output Waveforms of RL1872F. Above: Circuit of Figures 3, 4 and 6 (RC400/407). Below: With Charge Amplifier, Sample-and-Hold Circuit (RC400/407 plus CASH-IT).

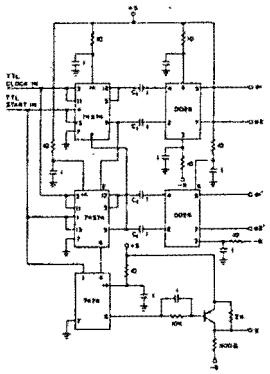


Figure 4. Four Phase Driver Circuit.

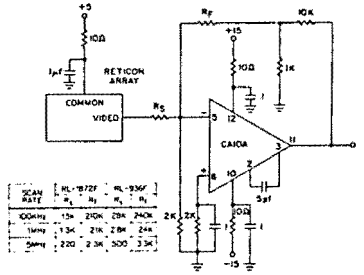


Figure 6. Simple Video Output Circuit Using CA-10A Op Amp.

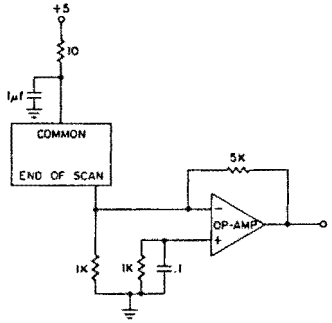


Figure 8. End-of-Scan Output Circuit.

The four clock phases and the properly timed start pulse S may be generated from TTL inputs using the drive circuit of Figure 4 which uses 0026 clock drivers. Good clock drivers are essential in order to minimize switching noise in the video output and to obtain maximum performance at high scan rates. The clock phases should have very fast rise and fall times with the rising edge of one phase matching the falling edge of another phase.

A timing diagram showing the clock and start waveforms generated by the circuits of Figures 3 and 4 and the corresponding video outputs is shown in Figure 5. It can be seen that a pair of diodes is sampled each time one of the clock phases makes a negative going transition. Alternate pairs of output pulses appear on video lines 1 and 2 and video lines 3 and 4. Note that although four separate outputs are provided, the timing is such that outputs 1 and 3 and outputs 2 and 4 may be shorted together and the video processed through only two channels.

If it is desired to process all four video outputs separately, two pairs of complimentary square wave clocks should be used in order to get optimum switching transient cancellation. These clocks should have leading edges identical to those of Figure 5, but the duty cycle should be 1/2 rather than 1/4 period. Timing of the video and end-of-scan outputs remains the same.

SIGNAL EXTRACTION

The video output of the RL-1872F is a train of 468 charge pulses per scan on each of the 4 video lines. The timing of the output pulses is shown in Figure 5. As mentioned above the outputs of the four video lines may be amplified separately or video 1 and 3, and 2 and 4, may be combined before amplification. If this is done only two output channels are necessary—one for the odd and one for the even elements.

Since the output of these arrays appears as a purely capacitive source, the video signals should be amplified using either current or charge amplifiers. Figure 6 shows a simple current amplifier which makes use of the RETICON CA10A op amp. Approximate resistor values for various scan rates are shown in the insert. Other op amps may be used provided they have a minimum open loop gain of 40 dB at the scan frequency and a slew rate (V/μsec) of at least 30 times the scan rate (MHz). The upper trace of Figure 7 shows an oscilloscope photograph of the output waveform expected from the RL-1872F using the circuits of Figures 3, 4 and 6. Greater dynamic range may be achieved at the expense of more complicated circuitry by filtering to remove switching transients or by using a charge amplifier/sample-and-hold circuit, such as the RETICON CASH-1T circuit module. The video output of this circuit is shown in the lower trace of Figure 7.

END OF SCAN

End-of-scan output pulses are provided when the last two pairs of diodes are sampled. These end-of-scan outputs are provided primarily for test purposes. When not in use they should be shorted externally to the +5 volt supply to avoid introduction of unwanted "glitches" into the video. In some applications, however, it may be desirable to use the end-of-scan outputs. In these cases, it is recommended that the voltage excursion on the end-of-scan pins be minimized by using a circuit such as that shown in Figure 8. The timing of the End-of-Scan output pulses is shown in Figure 5.

SENSOR GEOMETRY

The light sensitive area of the RL-1872F and the RL-936F is defined by a 16 micron (0.63 mil) wide aperture in a metal light shield on the silicon chip. The entire area within the aperture is light sensitive, i.e., there is no dead space between diodes. Therefore, the effective area of each sensor is 15 microns x 16 microns or 2.4 x 10^{-6} cm^2.

SENSITIVITY AND SPECTRAL RESPONSE

Since the RL-1872F and RL-936F operate in the charge storage mode, the output of each diode (below saturation) is proportional to exposure, i.e., the light intensity times the time interval between successive scans. Thus speed and sensitivity can be traded off, the longer the integration time the more sensitive the device. Integration time may be increased either by reducing the clock frequency or by delaying the start pulse. A plot of charge output versus exposure is shown in Figure 9.

Spectral response is typical of high quality diffused silicon photodiodes, covering the range from below 0.4 to 1.1 microns and peaking at about 0.8 microns. Typical spectral response and quantum efficiency curves are shown in Figure 10.

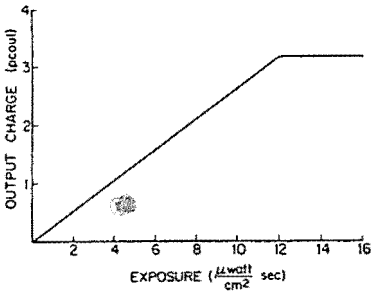


Figure 9. Signal Charge Per Cell as a Function of Exposure for a 2870°K Tungsten Light Source.

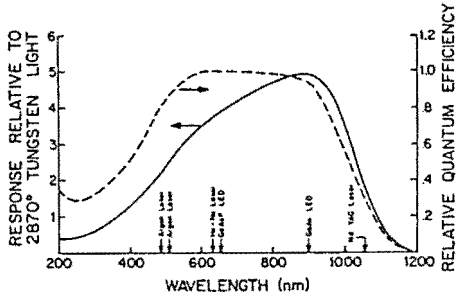


Figure 10. Dependence of Sensitivity and Quantum Efficiency on Wavelength.

CIRCUIT CARDS

Printed circuit cards containing all required drive and amplifier circuitry for operation of the RL1872F and the RL936F are available from Reticon and are highly recommended for first time array evaluation. A model RC400 mother board which contains clock and counter circuits and logic to generate four clock phases is required for either array. In addition, a model RC407 (RL1872F) or model RC406 (RL936F) driver/amplifier board is required. Each of these small boards contains clock drivers, two amplifiers for the odd and even channels and a socket for the array. The driver/amplifier board may be plugged into the mother board or remotely located up to 30 inches away. These boards provide video outputs similar to the upper trace of Figure 7.

The video may be further processed using a CASH-1T circuit which integrates, samples, and holds the video pulses in each channel. It then toggles between the two channels to recompose the video into a single boxcar output. The lower trace of Figure 7 is a typical output waveform from the CASH-1T.

The RC400, RC406, and RC407 will operate at sample rates up to 10MHz. The CASH-1T will only operate at sample rates up to 500KHz.

ELECTRICAL CHARACTERISTICS (25° C)

	Min	Typ	Max	Units
Positive Supply Voltage	—	+5	+8	Volts
Clock Amplitude (with Respect to Positive Supply)	-11	-12	-15	Volts
Start Pulse Amplitude (with Respect to Positive Supply)	-7.5	-12	-15	Volts
Clock Repetition Rate	—	—	10	MHz
Integration Time[1]	—	—	40	msec
Capacitance of Each Clock Line				
RL-1872F		100		pF
RL-936F		50		pF
Capacitance of Each Video Line (at 5V bias)				
RL-1872F		65		pF
RL-936F		33		pF
End-of-Scan Output Resistance		5		Kohm
Power Dissipation (DC)		4		mwatt

ELECTRO-OPTICAL CHARACTERISTICS

	RL-1872F	RL-936F	Units
Number of Sensors	1872	936	—
Center to Center Spacing	15	15	microns
Aperture Width	16	16	microns
Aperture Length	2.808	1.404	cm
Photodiode Sensitivity[2]	.26	.26	pAcm²/μwatt
Uniformity of Sensitivity[2]	12	10	±% typ
Saturation Exposure[2]	12.3	12.3	μwatt sec/cm²
Saturation Charge	3.2	3.2	pcoul

ABSOLUTE MAXIMUM RATINGS

	Min	Max	Units
Voltage with Respect to Common	0	-20	Volts
Storage Temperature	-55	+125	°C
Temperature under Bias	-55	+85	°C

[1]Devices can be operated with longer integration time but dark signal may increase to an objectionable level unless temperature is reduced. Dark signal changes by a factor of 2 every 7°C.

[2]For 2870° K tungsten light source.

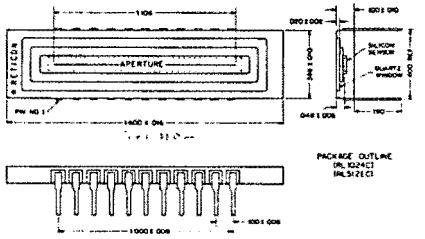


Figure 11. Outline Drawing of RL1872F.

Dimensions given in inches.

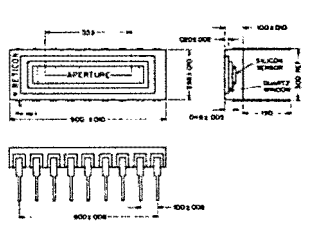


Figure 12. Outline Drawing of RL936F.

BURR-BROWN®

OPA101
OPA102

Low Noise - Wideband
PRECISION JFET INPUT OPERATIONAL AMPLIFIER

FEATURES

- GUARANTEED NOISE SPECTRAL DENSITY - 100% Tested
- LOW VOLTAGE NOISE - 8nV/$\sqrt{Hz}$ max at 10kHz
- LOW VOLTAGE DRIFT - 5μV/°C max (B grade)
- LOW OFFSET VOLTAGE - 250μV max (B grade)
- LOW BIAS CURRENTS - 10pA max at 25°C Ambient (B Grade)
- HIGH SPEED - 10V/μsec min (OPA102)
- GAIN BANDWIDTH PRODUCT - 40MHz (OPA102)

APPLICATIONS

- LOW NOISE SIGNAL CONDITIONING
- LIGHT MEASURMENTS
- RADIATION MEASUREMENTS
- PIN DIODE APPLICATIONS
- DENSITOMETERS
- PHOTODIODE/PHOTOMULTIPLIER CIRCUITS
- LOW NOISE DATA ACQUISITION

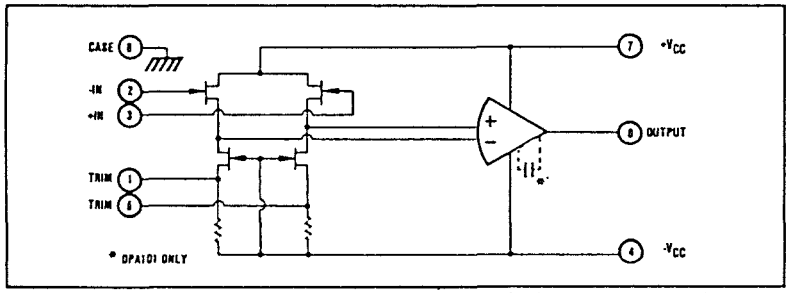
DESCRIPTION

The OPA101 and OPA102 are the first FET operational amplifiers available with noise characteristics (voltage spectral density) guaranteed and 100% tested.

The amplifiers have a complementary set of specifications permitting low errors in signal conditioning applications; low noise, low bias current, high open-loop gain, high common-mode rejection, low offset voltage, low offset voltage drift, etc.

In addition, the amplifiers have moderately high speed. The OPA101 is compensated for unity gain stability and has a slew rate of 5V/μsec, min. The OPA102 is compensated for gains of 3V/V and above and has a slew rate of 10V/μsec, min.

Each unit is laser-trimmed for low offset voltage and low offset voltage drift versus temperature. Bias currents are specified with the units fully warmed up at +25°C ambient temperature.



International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

SPECIFICATIONS

ELECTRICAL

Specifications at T_A = +25°C and $\pm V_{CC}$ = ±15VDC unless otherwise noted.

MODEL		OPA101/102AM			OPA101/102BM			
PARAMETER	CONDITION	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
INPUT NOISE								
Voltage Noise Density	f_o = 1Hz[1]		100	200		80	100	nV/$\sqrt{Hz}$
	f_o = 10Hz		32	60		25	30	nV/$\sqrt{Hz}$
	f_o = 100Hz		14	30		11	15	nV/$\sqrt{Hz}$
	f_o = 1kHz		9	15		8	12	nV/$\sqrt{Hz}$
	f_o = 10kHz		7	8		7	8	nV/$\sqrt{Hz}$
	f_o = 100kHz		6.5	8		6.5	8	nV/$\sqrt{Hz}$
f_c; 1/f Corner Frequency			125			100		Hz
Voltage Noise	f_B = 0.1Hz to 10Hz[1]		1.3	2.6		1.0	1.3	μV, p-p
	f_B = 10Hz to 10kHz		1.0	1.2		0.8	1.0	μV, rms
	f_B = 10Hz to 100kHz		2.1	2.6		2.1	2.6	μV, rms
Current Noise Density	f_o = 0.1Hz thru 10kHz		2.0			1.4		fA/$\sqrt{Hz}$
Current Noise	f_B = 0.1Hz to 10Hz		38			26		fA, p-p
	f_B = 10Hz to 10kHz		200			140		fA, rms
DYNAMIC RESPONSE								
Bandwidth, Unity Gain	Small Signal							
OPA101			10			•		MHz
OPA102			Note 2			•		
Gain-Bandwidth Product	A_{CL} = 100							
OPA101			20			•		MHz
OPA102			40			•		MHz
Full Power Bandwidth	V_o = 20V, p-p; R_L = 1kΩ							
OPA101		80	100		•	•		kHz
OPA102		160	210		•	•		kHz
Slew Rate	V_o = ±10V; R_L = 1kΩ							
OPA101	A_{CL} = -1	5	6.5		•	•		V/μsec
OPA102	A_{CL} = -3	10	14		•	•		V/μsec
Settling Time (OPA101)	V_o = ±5V; A_{CL} = -1; R_L = 1kΩ							
ε = 1%			2			•		μsec
ε = 0.1%			2.5			•		μsec
ε = 0.01%			10			•		μsec
Settling Time (OPA102)	V_o = ±5V; A_{CL} = -3; R_L = 1kΩ							
ε = 1%			1			•		μsec
ε = 0.1%			1.5			•		μsec
ε = 0.01%			8			•		μsec
Small-Signal Overshoot	R_L = 1kΩ; C_L = 100pF							
OPA101	A_{CL} = +1		15			•		%
OPA102	A_{CL} = +3		20			•		%
Rise Time	10% to 90%, Small Signal							
OPA101			40			•		nsec
OPA102			30			•		nsec
Phase Margin	R_L = 1kΩ							
OPA101	A_{CL} = +1		60			•		Degrees
OPA102	A_{CL} = +3		45			•		Degrees
Overload Recovery[3]								
OPA101	A_{CL} = -1, 50% overdrive		1			•		μsec
OPA102	A_{CL} = -3, 50% overdrive		0.8			•		μsec
OPEN-LOOP GAIN, DC								
Full Load	V_o = ±10V; R_L = 1kΩ	94	105		•	•		dB
No Load	V_o = ±10V; R_L ≥ 10kΩ	96	108		•	•		dB
RATED OUTPUT								
Voltage	I_o = ±12mA	±12	±13		•	•		V
Current	V_o = ±12V	±12	±30		•	•		mA
Output Resistance	Open-Loop, f = DC		500			•		Ω
Short-Circuit Current			±45			•		mA
Capacitive Load Range	Phase Margin ≥ 25°							
OPA101	A_{CL} = +1		500			•		pF
OPA102	A_{CL} = +3		300			•		pF
INPUT OFFSET VOLTAGE								
Initial Offset	T_A = +25°C		±100	±500		±50	±250	μV
vs Temperature	-25°C ≤ T_A ≤ +85°C		±6	±10		±3	±5	μV/°C
vs Supply Voltage	±5VDC ≤ | V_{CC} | ≤ ±20VDC		±10	±50		•	•	μV/V
vs Time			±10			•		μV/mo
Adjustment Range	Circuit in "Connection Diagram"		±1			•		mV
INPUT BIAS CURRENT								
Initial Bias	T_A = +25°C		-12	-15		-6	-10	pA
vs Temperature			Note 4			•		
vs Supply Voltage			Note 5			•		

ELECTRICAL (CONT)

MODEL		OPA101/102AM			OPA101/102BM			
PARAMETER	CONDITION	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
INPUT DIFFERENCE CURRENT								
Initial Difference	T_A = +25°C		±3	±6		±1.5	±4	pA
vs Temperature			Note 4			*		
vs Supply Voltage			Note 5			*		
INPUT IMPEDANCE								
Differential								
Resistance			10^{12}			*		Ω
Capacitance			1			*		pF
Common-mode								
Resistance			10^{13}			*		Ω
Capacitance			3			*		pF
INPUT VOLTAGE RANGE								
Common-mode Voltage Range	Linear Operation		± [Vcc] -3			*		V
Common-mode Rejection	f_O = DC, V_{CM} = ±10V	80	105		*	*		dB
POWER SUPPLY								
Rated Voltage			±15			*		VDC
Voltage Range	Derated Performance	±5		±20	*	*	*	VDC
Current, Quiescent			5.8	8		*	*	mA
TEMPERATURE RANGE								
Specification		-25		+85	*		*	°C
Operating	Derated Performance	-55		+125	*		*	°C
Storage		-65		+150	*		*	°C

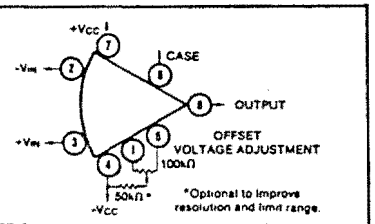
NOTES. *Specifications same as for OPA101/102AM.
1. Parameter is untested and is not guaranteed. This specification is established to a 90% confidence level.
2. Minimum stable gain for the OPA102 is 3V/V
3. Time required for output to return from saturation to linear operation following the removal of an input overdrive signal.
4. Doubles approximately every 8.5°C.
5. See Typical Performance Curves.

ABSOLUTE MAXIMUM RATINGS

Supply	±20VDC
Internal Power Dissipation[1]	750mW
Differential Input Voltage[2]	±20VDC
Input Voltage, Either Input[2]	±20VDC
Storage Temperature Range	-65°C to +150°C
Operating Temperature Range	-55°C to +125°C
Lead Temperature (soldering, 10 seconds)	+300°C
Output Short-Circuit Duration[3]	60 seconds
Junction Temperature	+175°C

NOTES:
1. Package must be derated according to the details in the Application Information section.
2. For supply voltages less than ±20VDC, the absolute maximum input is equal to the supply voltage.
3. Short-circuit may be to ground only. See discussion of Thermal Model in the Application Information section.

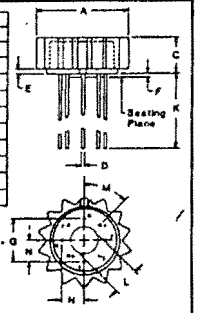
CONNECTION DIAGRAM



NOTE: Offset voltage adjustment affects voltage drift vs temperature by approximately ±0.3μV/°C for each 100μV of offset adjusted

MECHANICAL SPECIFICATIONS

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.488	.522	12.42	13.26
C	.243	.307	6.17	7.80
D	.016	.021	0.41	0.53
E	.010	.040	0.25	1.02
F	.010	.040	0.25	1.02
G	.200	BASIC	5.08	BASIC
K	.500	--	12.7	--
L	.110	.160	2.79	4.06
M	45°	BASIC	45°	BASIC
N	.095	.105	2.41	2.67



NOTE:
Leads in true position within .010" (.25mm) R at MMC at seating plane.

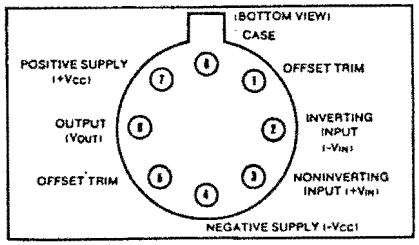
Pin numbers shown for reference only. Numbers may not be marked on package.

Pin material and plating composition conform to method 2003 (solderability) of MIL-STD-883 (except paragraph 3.2).

Weight: 2 grams

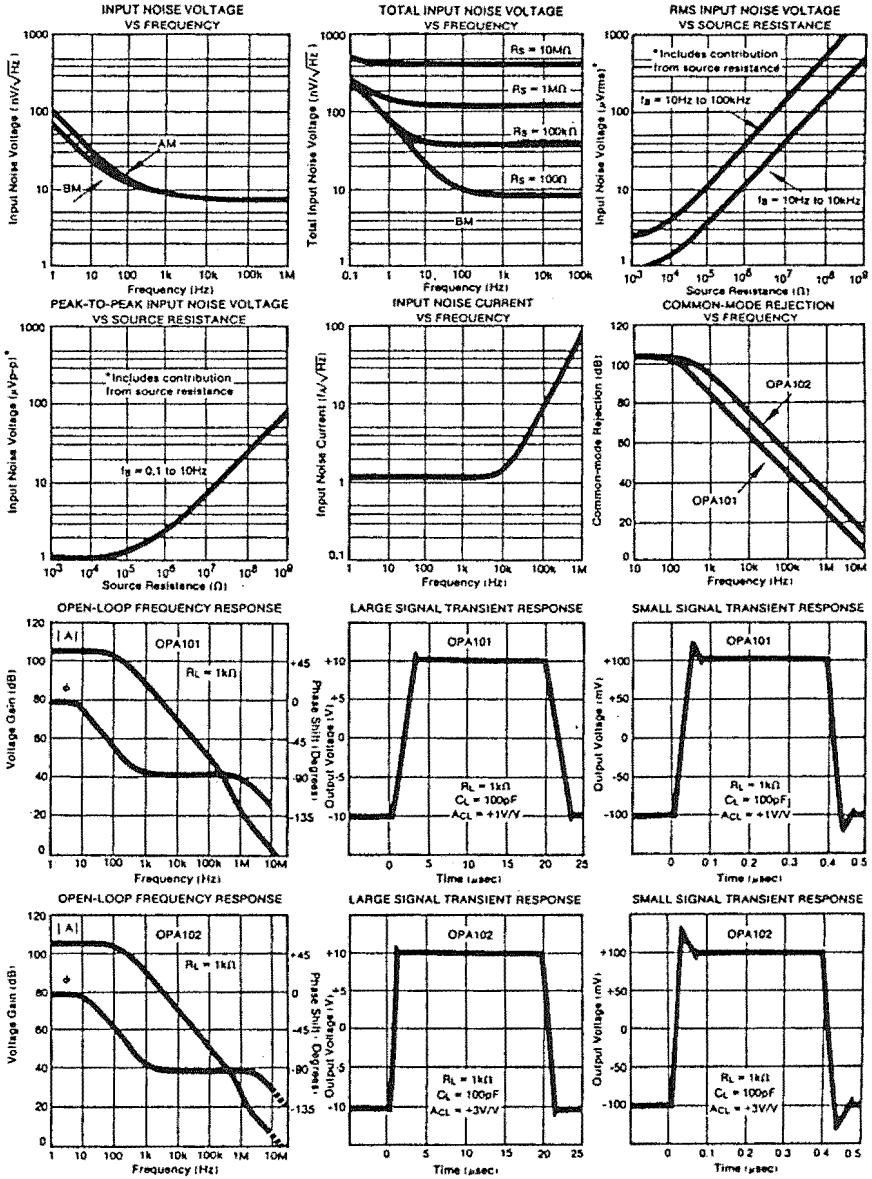
Order Number:
OPA101AM OPA101BM
OPA102AM OPA102BM

PIN CONFIGURATION

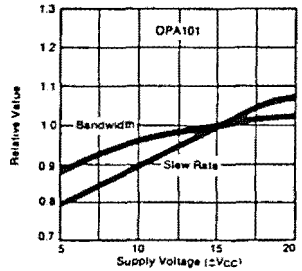


TYPICAL PERFORMANCE CURVES

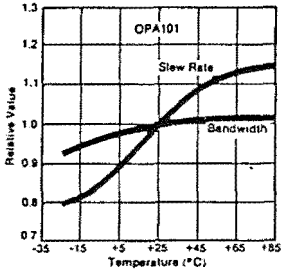
(T_A = +25°C, ±Vcc = ±15VDC, unless otherwise noted. Performance curves apply to both OPA101 and OPA102 unless otherwise noted.)



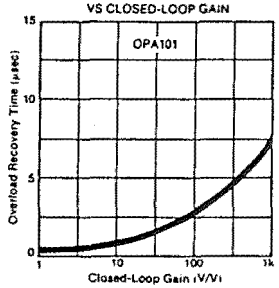
FREQUENCY CHARACTERISTICS VS SUPPLY VOLTAGE



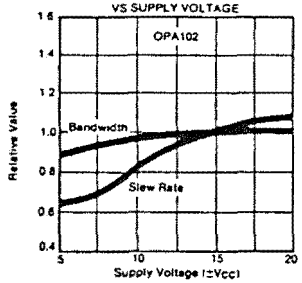
FREQUENCY CHARACTERISTICS VS AMBIENT TEMPERATURE



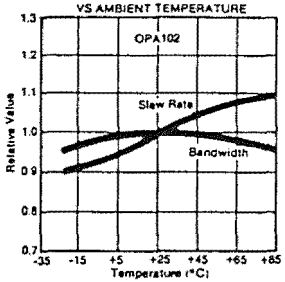
OVERLOAD RECOVERY TIME VS CLOSED-LOOP GAIN



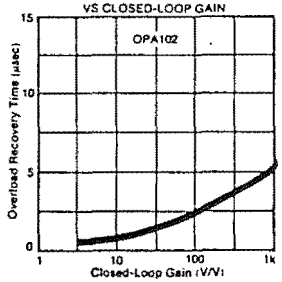
FREQUENCY CHARACTERISTICS VS SUPPLY VOLTAGE



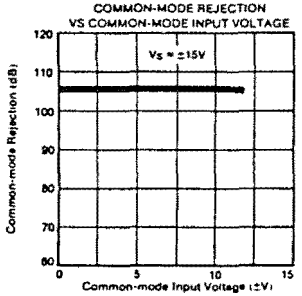
FREQUENCY CHARACTERISTICS VS AMBIENT TEMPERATURE



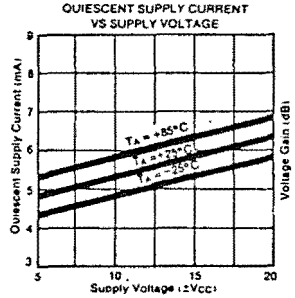
OVERLOAD RECOVERY TIME VS CLOSED-LOOP GAIN



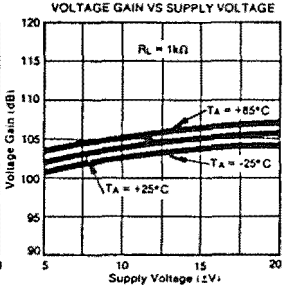
COMMON-MODE REJECTION VS COMMON-MODE INPUT VOLTAGE



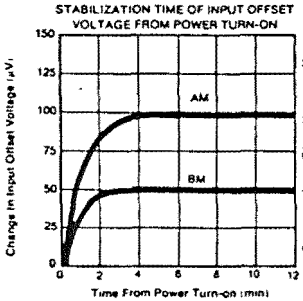
QUIESCENT SUPPLY CURRENT VS SUPPLY VOLTAGE



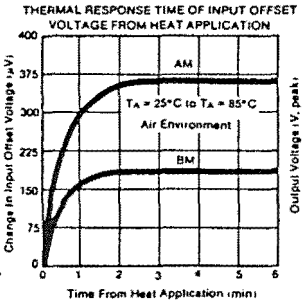
VOLTAGE GAIN VS SUPPLY VOLTAGE



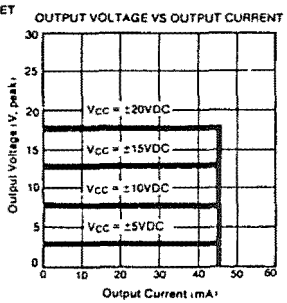
STABILIZATION TIME OF INPUT OFFSET VOLTAGE FROM POWER TURN-ON



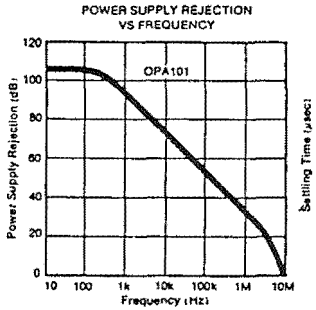
THERMAL RESPONSE TIME OF INPUT OFFSET VOLTAGE FROM HEAT APPLICATION



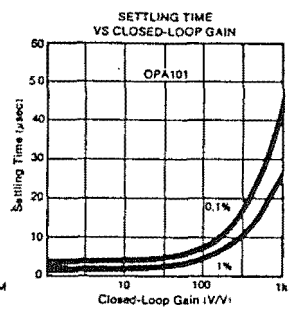
OUTPUT VOLTAGE VS OUTPUT CURRENT



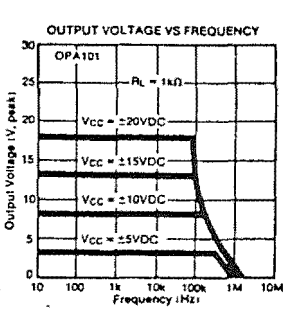
POWER SUPPLY REJECTION VS FREQUENCY



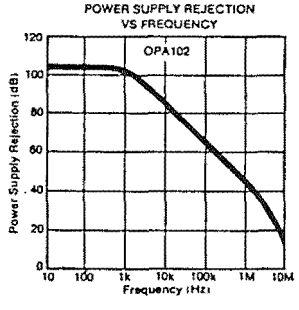
SETTLING TIME VS CLOSED-LOOP GAIN



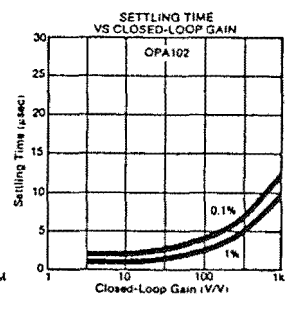
OUTPUT VOLTAGE VS FREQUENCY



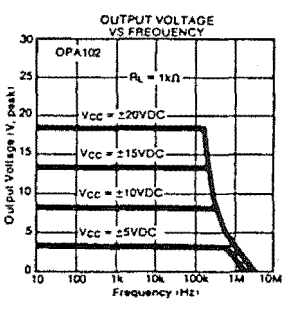
POWER SUPPLY REJECTION VS FREQUENCY



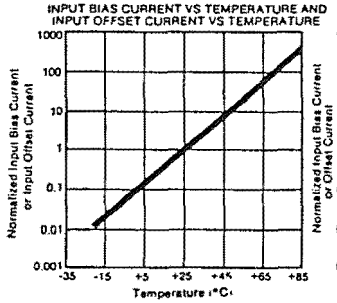
SETTLING TIME VS CLOSED-LOOP GAIN



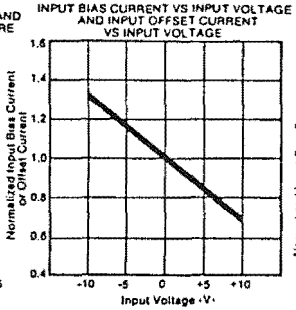
OUTPUT VOLTAGE VS FREQUENCY



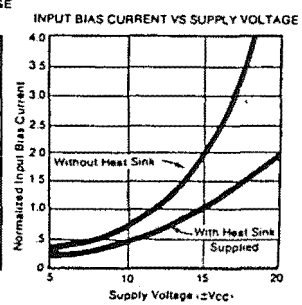
INPUT BIAS CURRENT VS TEMPERATURE AND INPUT OFFSET CURRENT VS TEMPERATURE



INPUT BIAS CURRENT VS INPUT VOLTAGE AND INPUT OFFSET CURRENT VS INPUT VOLTAGE



INPUT BIAS CURRENT VS SUPPLY VOLTAGE



APPENDIX EIGHT

THE AMD Am9513 SYSTEM TIMING CONTROLLERS [1]

The operating philosophy of the Am9513 is based on the use of general-purpose counters that can be controlled in various ways to produce the functions desired. Broadly, use of the counters falls into two classic categories: (a) count accumulation, and (b) frequency division.

In the first case, the counter simply accumulates a count of transitions that occur on its input. An output that indicates the zero state of the counter would be of only incidental interest. The counter value should be available at any time to the associated CPU or it might be compared with some independent value. The accumulated count might be modified or the counter input conditioned by various controls, including hardware and software gating functions; in any event, in these types of applications, it is the value of the actual count that is of interest.

In the case of frequency division, on the other hand, it is an output waveform that is of interest and the counter input information may be incidental. With an output signal that indicates the zero state of the counter, selection of the effective length of the counter and the input frequency are controlled to provide the desired output frequency. Additional controls may allow various types of output waveforms to be generated from the base output frequency, but the actual counter value will usually not be of direct interest.

The Am9513 has been designed to handle effectively both modes of operation, even intermixed on the same chip. In many instances, of course, both types of counter usage will be combined to provide the desired function.

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[1] from Advanced Micro Devices: Am9513A/Am9513 System Timing Controller Technical Manual (1984), Chapter 1.

FUNCTIONAL DESCRIPTION

The Am9513 System Timing Controller (STC) is a support device for processor oriented systems that is designed to enhance the available capability with respect to counting and timing operations. It provides the capability for programmable frequency synthesis, high resolution programmable duty cycle waveforms, retriggerable digital timing functions, time-of-day clocking, coincidence alarms, complex pulse generation, high resolution baud rate generation, frequency shift keying, stop-watching timing, event count accumulation, waveform analysis and many more. A variety of programmable operating modes and control features allow the AM9513 to be personalized for particular applications as well as dynamically reconfigured under programme control.

The STC includes five general-purpose 16-bit counters. A variety of internal frequency sources and external pins may be selected as inputs for individual counters with software selectable active-high or active-low input polarity. Both hardware and software gating of each counter is available. Three-state outputs for each counter provide either pulses or levels. The counters can be programmed to count up or down in either binary or BCD. The accumulated count may be read without disturbing the counting process. Any of the counters may be internally concatenated to form an effective counter length of up to 80 bits.

The Am9513 block diagrams (figures A8.1, A8.2 and A8.3) indicate the interface signals and the basic flow of information. Internal control lines and the internal data bus have been omitted. The control and data registers are all connected to a common internal 16-bit bus. The external bus may be 8- or 16-bits wide; in the 8-bit mode the internal 16-bit information is multiplexed to the low order byte of the data bus.

An internal oscillator provides a convenient source of frequencies for use as counter inputs. The oscillator's frequency is controlled at the X1 and X2 interface pins by an external reactive network such as a crystal. The oscillator output is divided by the Frequency Scalar to provide several

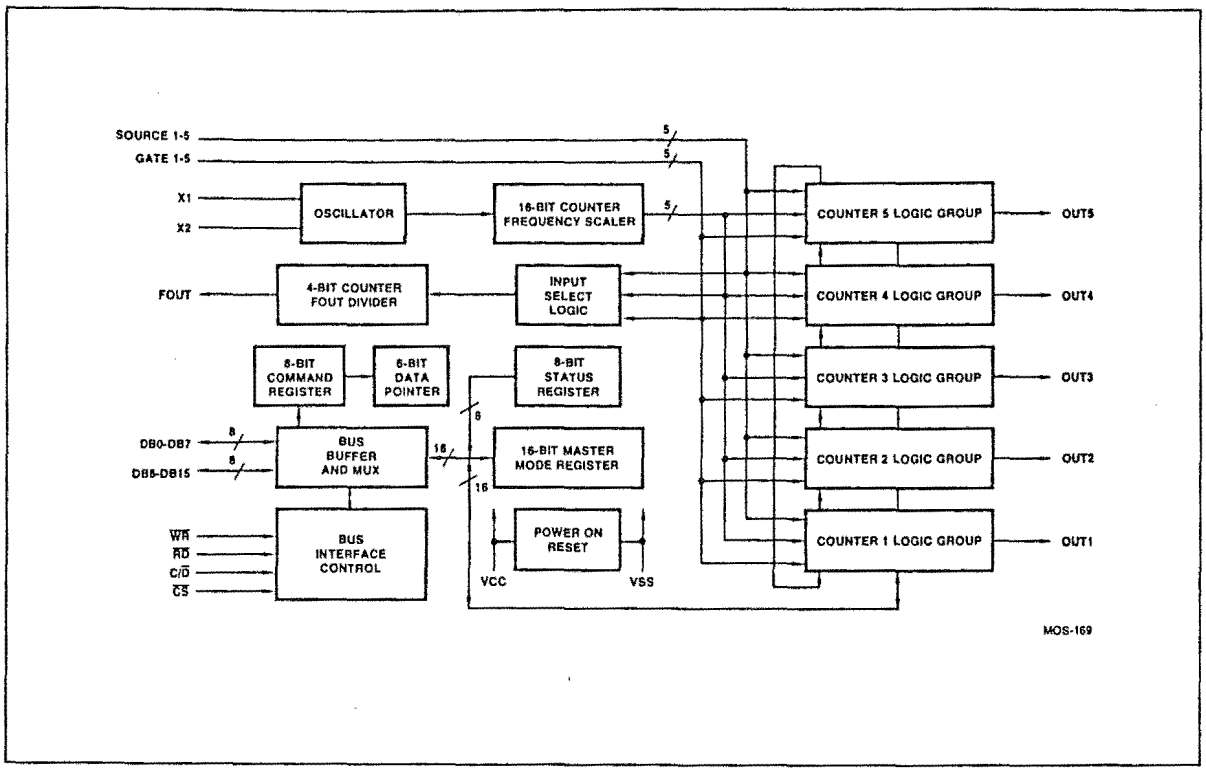


Figure A8.1: General block diagram for an Am9513 STC.

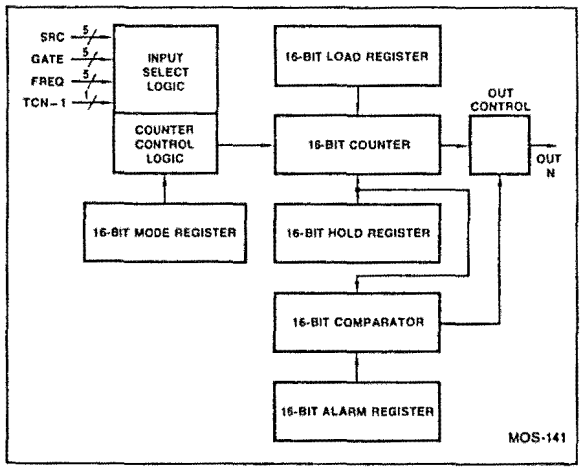


Figure A8.2: Counter logic groups 1 and 2.

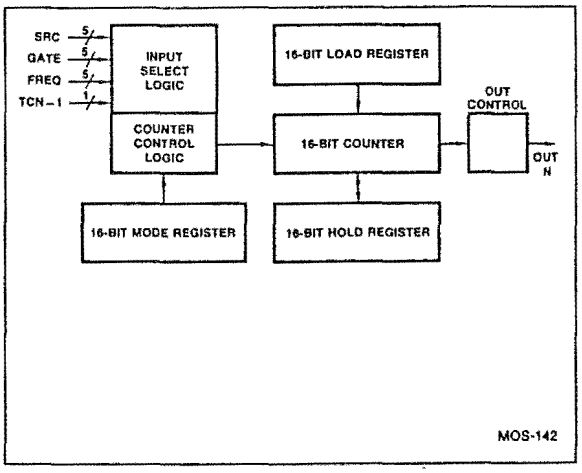


Figure A8.3: Counter logic groups 3, 4 and 5.

sub-frequencies. One of the scaled frequencies (or one of ten input signals) may be selected as an input to the FOUT divider and then comes out of the chip at the FOUT interface pin.

The STC is addressed by the external system as two locations: a Control port and a Data port. The Control port provides direct access to the Status and Command registers, as well as allowing the user to update the Data Pointer register.

The Data port is used to communicate with all other addressable internal locations. The Data Pointer register controls the Data port addressing.

Among the registers accessible through the Data port are the Master Mode register and five Counter Mode registers, one for each counter. The Master Mode register controls the programmable options that are not controlled by the Counter Mode registers.

Each of the five general-purpose counters is 16-bits long and is independently controlled by its Counter Mode register. Through this register a user can software select one of 16 sources as the counter input, a variety of gating and repetition modes, up or down counting in binary or BCD and active-high or active-low input and output polarities.

Associated with each counter are a Load register and a Hold register, both accessible through the Data port. The Load register is used to automatically reload the counter to any predefined value, thus controlling the effective count period. The Hold register is used to save count values without disturbing the count process, permitting the host processor to read intermediate counts. In addition, the Hold register may be used as a second Load register to generate a number of complex output waveforms.

All five counters have the same basic control logic and control registers. Counters 1 and 2 have additional Alarm registers and comparators associated with them, plus the extra logic necessary for operating in a 24-hour time-of-day mode. For real-time operation the time-of-day logic will accept 50Hz, 60Hz or 100Hz input frequencies.

Each general counter has a single dedicated output pin. It may be turned off when the output is not of interest or may be configured in a variety of ways to drive interrupt controllers, Darlington buffers, bus drivers, etc. The counter inputs, on the other hand, are specifically not dedicated to any given interface line. Considerable versatility is available for configuring both the input and the gating of individual counters. This not only permits dynamic reassignment of inputs under software control, but also allows multiple counters to use a single input and allows a single gate pin to control more than one counter. Indeed, a

single pin can be the gate for one counter, and, at the same time, the count source for another.

A powerful command structure simplifies user interaction with the counters. A counter must be armed by one of the ARM commands before counting can commence. Once armed, the counting process may be further enabled or disabled using the hardware gating facilities. The ARM and DISARM commands permit software gating of the count process in some modes.

The LOAD command causes the counter to be reloaded with the value in either the associated Load register or the associated Hold register. It will often be used as a software retrigger or as counter initialization prior to active hardware gating.

The DISARM command disables further counting independent of any hardware gating. A disarmed counter may be reloaded using the LOAD command, may be incremented or decremented using the STEP command, and may be read using the SAVE command. A count process may be resumed using an ARM command.

The SAVE command transfers the contents of a counter to its associated Hold register. This command will overwrite any previous Hold register contents. The SAVE command is designed to allow an accumulated count to be preserved so that it can be read by the host CPU at some later time.

Two combinations of the basic commands exist to either LOAD AND ARM or to DISARM AND SAVE any combination of counters. Additional commands are provided to: step an individual counter by one count; set and clear an output toggle; issue a software reset; clear and set special bits in the Master Mode register; and load the Data Pointer register.

Note: Separate LOAD and ARM commands should be used for asynchronous operations.

OUTPUT CONTROL

Counter mode bits CM0 through CM2 specify the output control configuration. Figure A8.4 shows a schematic representation of the output control logic. The OUT pin may

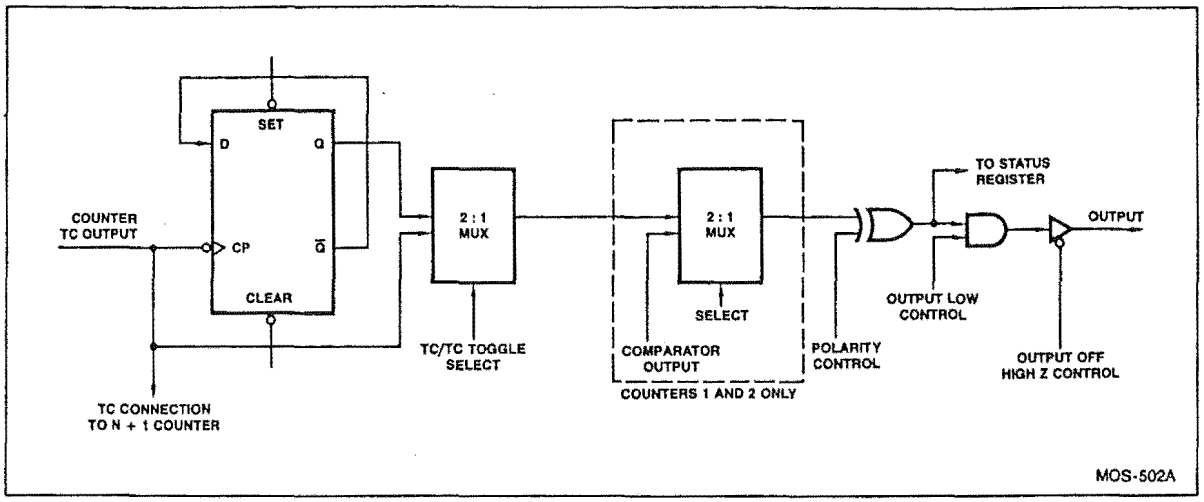


Figure A8.4: Output control logic.

be off (a high impedance state), or it may be inactive with a low impedance to ground. The three remaining valid combinations represent the active High, active Low or TC Toggle output waveforms.

One output form available is called Terminal Count (TC) and represents the period in time that the counter reaches an equivalent value of zero. TC will occur on the next count when the counter is at 0001 for down counting, at 9999 (BCD) for BCD up counting or at FFFF (hex) for binary up counting. Figure A8.5 shows a Terminal Count pulse and an example context that generated it. The TC width is determined by the period of the counting source. Regardless of any gating input or whether the count is Armed or Disarmed, the terminal count will go active for only one clock cycle. Figure A8.5 assumes active-high source polarity, counter armed, counter decrementing and an external reload value of K.

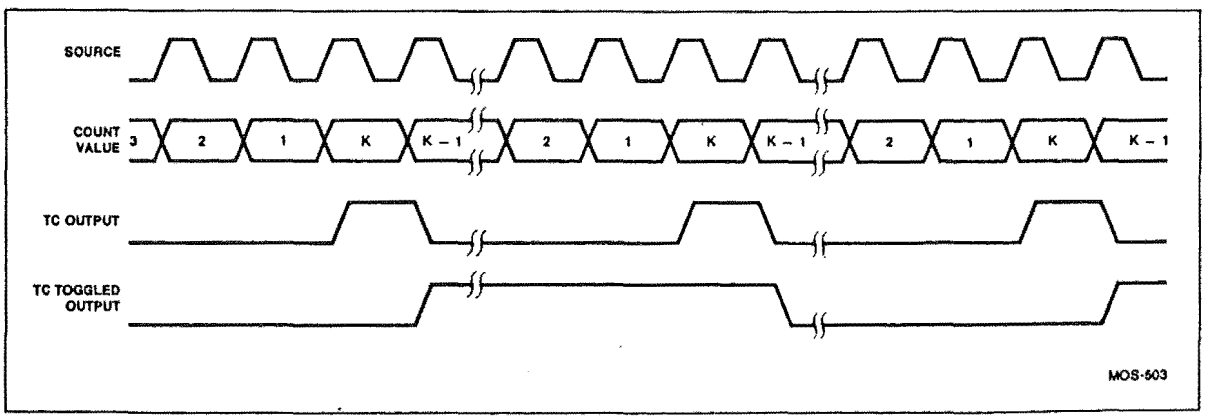


Figure A8.5: Counter output waveforms.

The counter will always be loaded from an external location when TC occurs; the user can choose the source location and the value. If a non-zero value is picked, the counter will never really attain a zero state and TC will indicate the counter state that would have been zero had no parallel transfer occurred.

The other output form, TC Toggled, uses the trailing edge of TC to toggle a flip-flop to generate an output level instead of a pulse. The toggle output is 1/2 the frequency of TC. The TC Toggled output will frequently be used to generate variable duty-cycle square waves in Operating Modes G through K.

In Mode L the TC Toggled output can be used to generate a one-shot function, with the delay to the start of the output pulse and the width of the output pulse separately programmable. With selection of the minimum delay to the start of the pulse, the output will toggle on the source pulse following application of the triggering Gate edge.

COUNTER MODE DESCRIPTIONS

Bits within the counter mode register select the operating mode for each counter. To simplify references to a particular mode, each mode is assigned a letter from A through X. Representative waveforms for the counter modes used in this detector are illustrated in figures A8.6 through A8.10. The figures assume down counting on rising source edges. Those modes which automatically disarm the counter are shown with the $\overline{WR}$ pulse entering the required ARM command; for modes which count repetitively the ARM command is omitted. The retriggering mode Q is shown with one retrigger operation. Both a TC output waveform and a TC Toggled output waveform are shown for each mode. The symbols L and H are used to represent count values equal to the Load and Hold register contents, respectively. The symbols K and N represent arbitrary count values. These figures are designed to clarify the mode descriptions; the Am9513 Electrical Specification should be used as the authoritative reference for timing relationships between signals. Appendix B providces a key to

the waveform symbols used in these diagrams.

To keep the following mode descriptions concise and to the point, the phrase "source edges" is used to refer to active-going source edges only, not to inactive-going edges. Similarly, the phrase "gate edges" refers only to active-going gate edges. Also, again to avoid verbosity and euphuism, the descriptions of some modes state that a counter is stopped or disarmed "on a TC, inhibiting further counting". As is fully explained in the TC section of this document, for these modes the counter is actually stopped or disarmed following the active-going source edge which drives the counter out of TC. In other words, since a count in the TC state always counts, irrespective of its gating or arming status, the stopping or disarming of the count sequence is delayed until TC is terminated.

MODE D

Rate Generator with No Hardware Gating

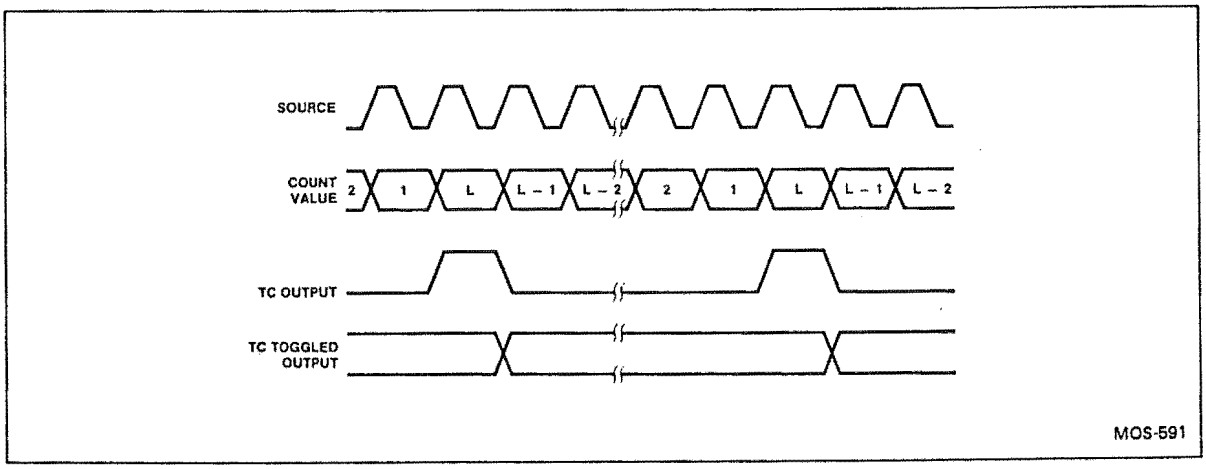


Figure A8.6: STC mode D waveforms.

Mode D, shown in figure A8.6, is typically used in frequency generation applications. In this mode, the Gate input does not affect counter operation. Once armed, the counter will count to TC repetitively. On each TC the counter will reload itself from the Load register; hence the Load register value determines the time between TCs. A square wave rate generator may be obtained by specifying the TC Toggled output mode in the Counter Mode register.

MODE G

Software-Triggered Delayed Pulse One-Shot

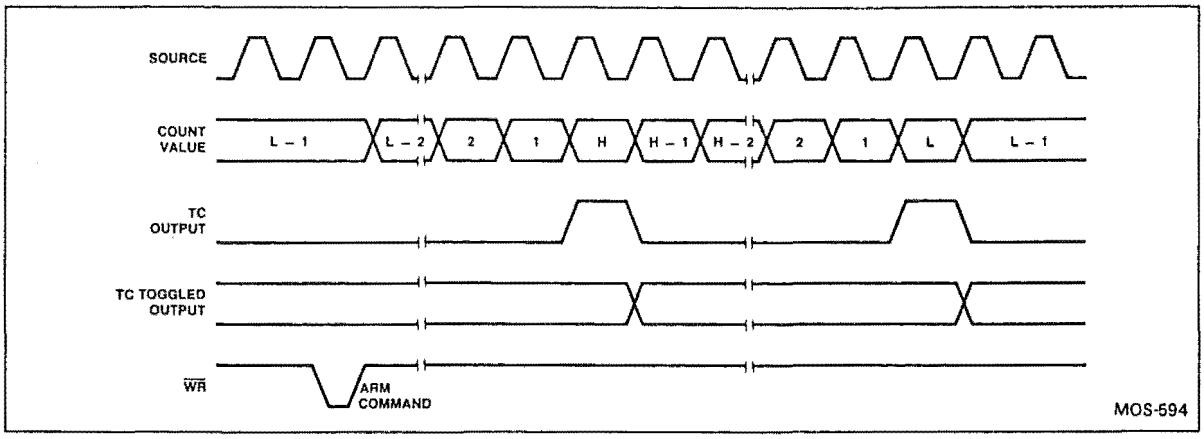


Figure A8.7: STC mode G waveforms.

In Mode G, shown in figure A8.7, the Gate does not affect the counter's operation. Once armed, the counter will count to TC twice and then automatically disarm itself. For most applications, the counter will initially be loaded from the Load register either by a LOAD command or by the last TC of an earlier timing cycle. Upon counting to the first TC, the counter will reload itself from the Hold register. Counting will proceed until the second TC, when the counter will reload itself from the Load register and automatically disarm itself, inhibiting further counting. Counting can be resumed by issuing a new ARM command. A software-triggered delayed pulse one-shot may be generated by specifying the TC Toggled output mode in the Counter Mode register. The initial counter contents control the delay from the ARM command until the output pulse starts. The Hold register contents control the pulse duration.

MODE I

Hardware-Triggered Delayed Pulse Strobe

Mode I, shown in figure A8.8, is identical to Mode G, except that counting will not begin until a Gate edge is applied to an armed counter. The counter must be armed before application of the triggering Gate edge; Gate edges applied to a disarmed counter are disregarded. An armed counter will

start counting on the first source edge after the triggering Gate edge. Counting will then proceed in the same manner as in Mode G. After the second TC, the counter will disarm itself. An ARM command and Gate edge must be issued in this order to restart counting. Note that after application of a triggering Gate edge, the Gate input will be disregarded until the second TC. This differs from Mode H, where the Gate can be modulated throughout the count cycle to stop and start the counter.

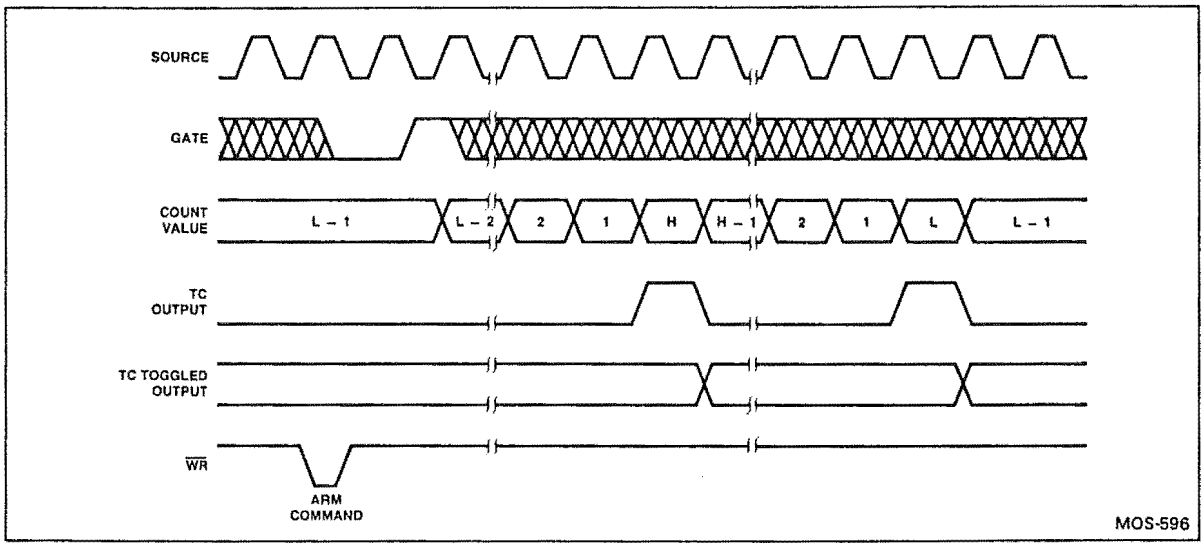


Figure A8.8: STC mode I waveforms.

MODE J

Variable Duty Cycle Rate Generator with No Hardware Gating

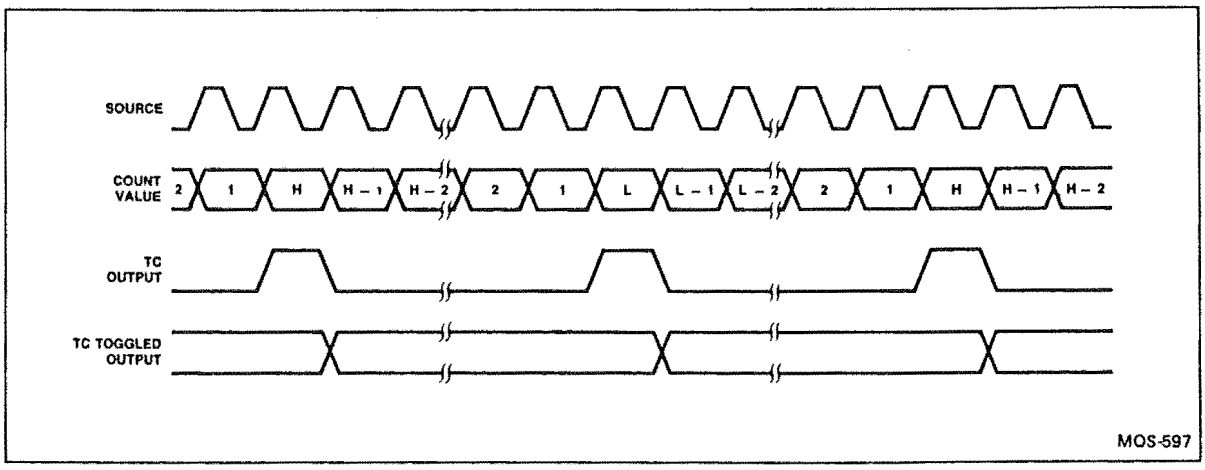


Figure A8.9: STC mode J waveforms.

Mode J, shown in Figure A8.9, will find the greatest usage in frequency generation applications with variable duty

cycle requirements. Once armed, the counter will count continuously until it is issued a DISARM command. On the first TC, the counter will be reloaded from the Hold register. Counting will then proceed until the second TC at which time the counter will be reloaded from the Load register. Counting will continue, with the reload source alternating on each TC, until a DISARM command is issued to the counter. (The third TC reloads from the Hold register, the fourth TC reloads from the Load register, etc.). A variable duty cycle output can be generated by specifying the TC Toggled output in the Counter Mode register. The Load and Hold values then directly control the output duty cycle, with high resolution available when relatively high count values are used.

MODE Q

Rate Generator with Synchronization (Event Counter with Auto-Read/Reset)

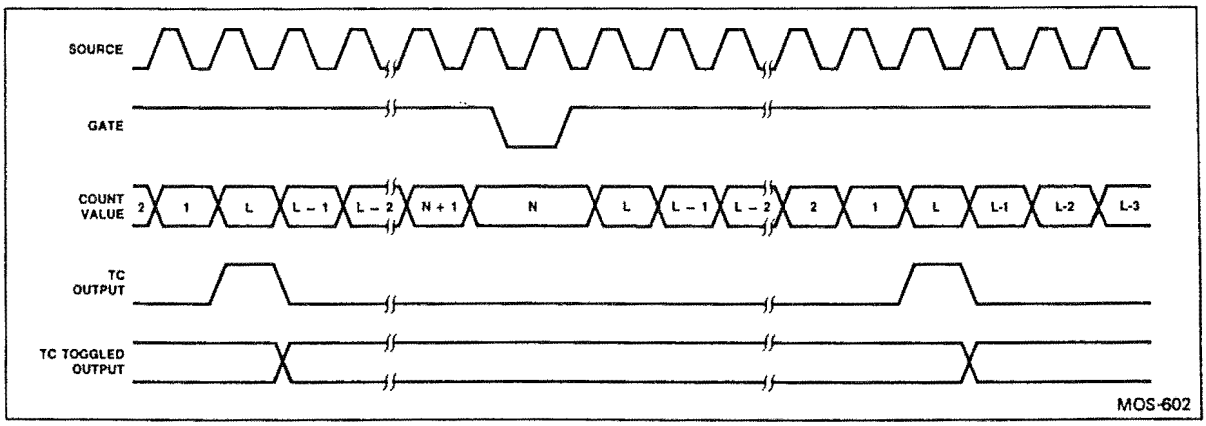


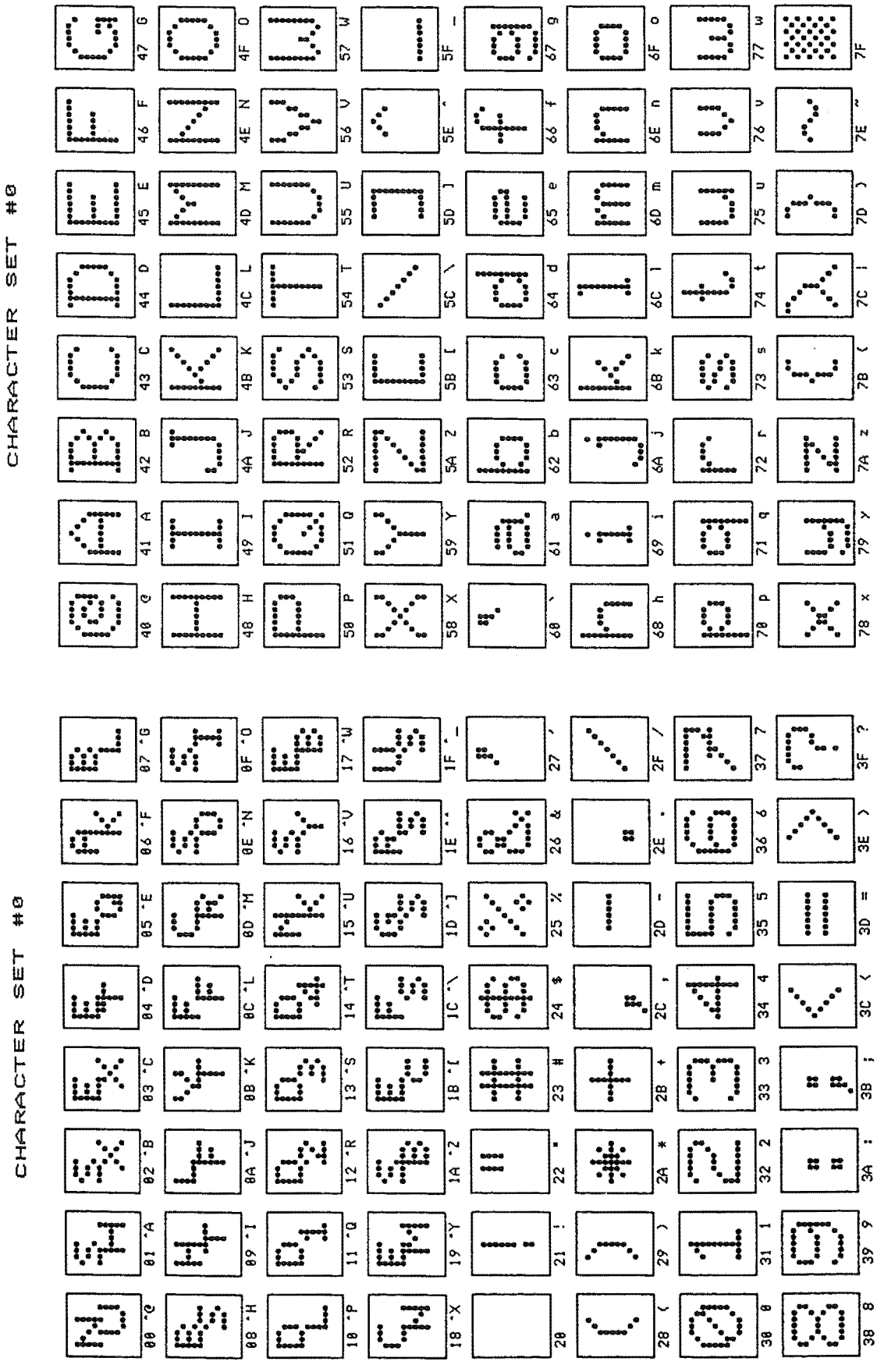
Figure A8.10: STC mode Q waveforms.

Mode Q, shown in figure A8.10, provides a rate generator with synchronization or an event counter with auto-read/reset. The counter must first be issued an ARM command before counting can occur. Once armed, the counter will count all source edges which occur while the Gate is active and disregard those edges which occur while the Gate is inactive. This permits the Gate to turn the count process on and off. After the issuance of an ARM command and the application of an active Gate, the counter will count to TC repetitively. On each TC the counter will reload itself from

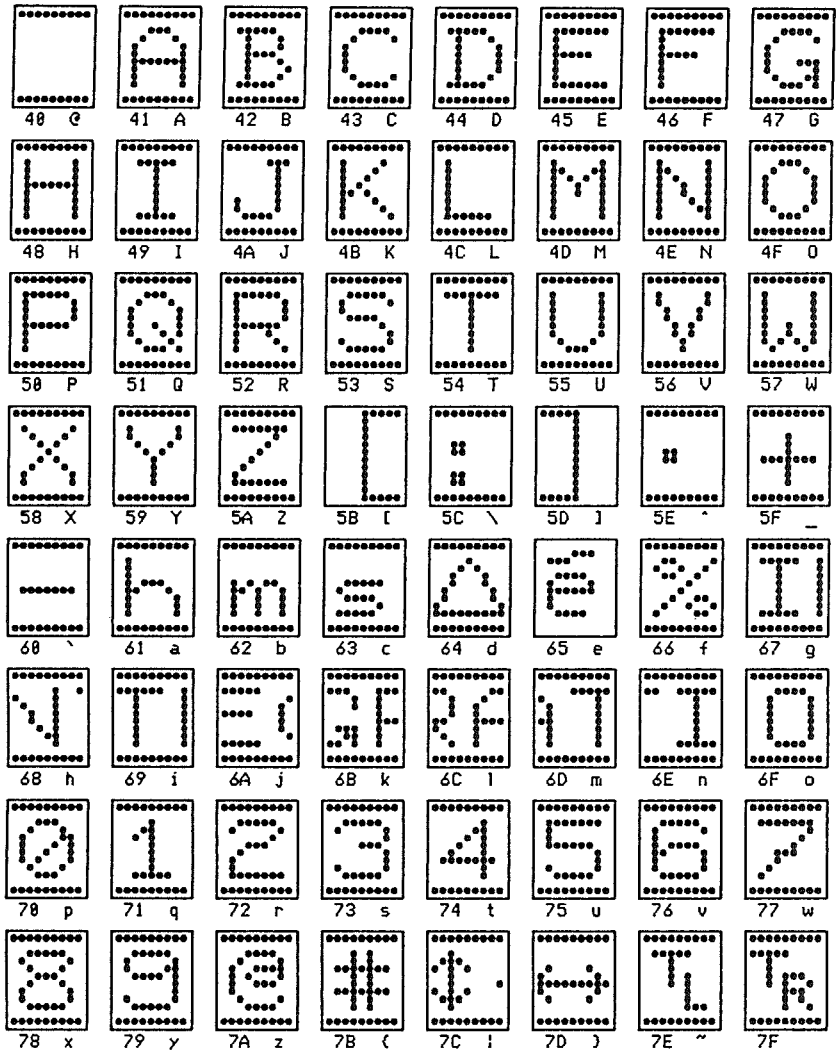
the Load register. The counter may be retriggered at any time by presenting an active-going Gate edge to the Gate input. The retriggering Gate edge will transfer the contents of the counter into the Hold register. The first qualified source edge after the retriggering Gate edge will transfer the contents of the Load register in the Counter. Counting will resume on the second qualified source edge after the retriggering gate edge. Qualified source edges are active-going edges which occur while the Gate is active.

APPENDIX NINE

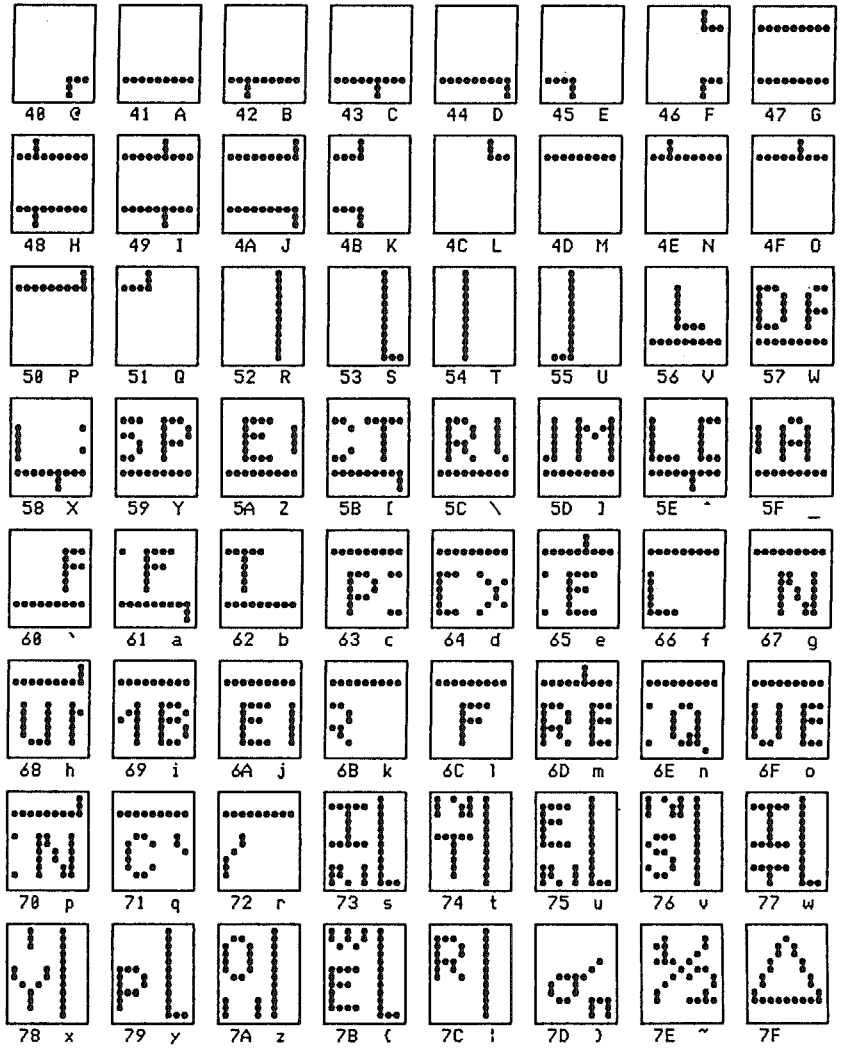
THE TERMINAL CUSTOM CHARACTER SETS



CHARACTER SET #1



CHARACTER SET #2



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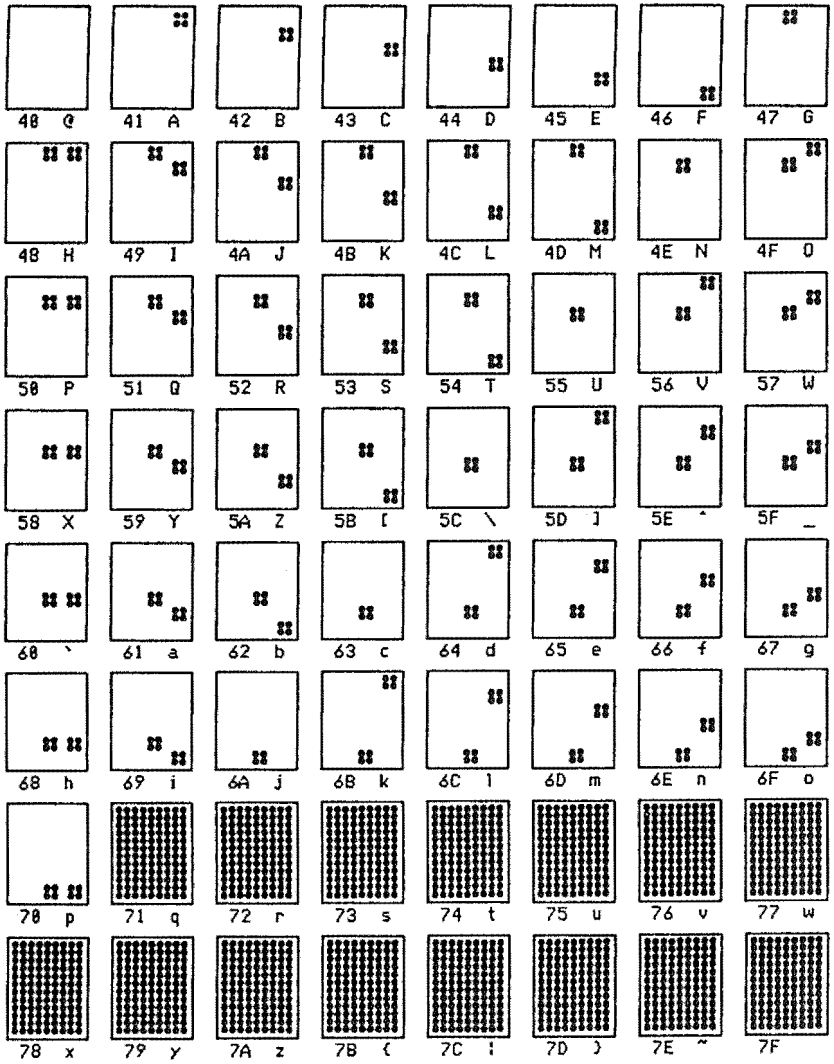

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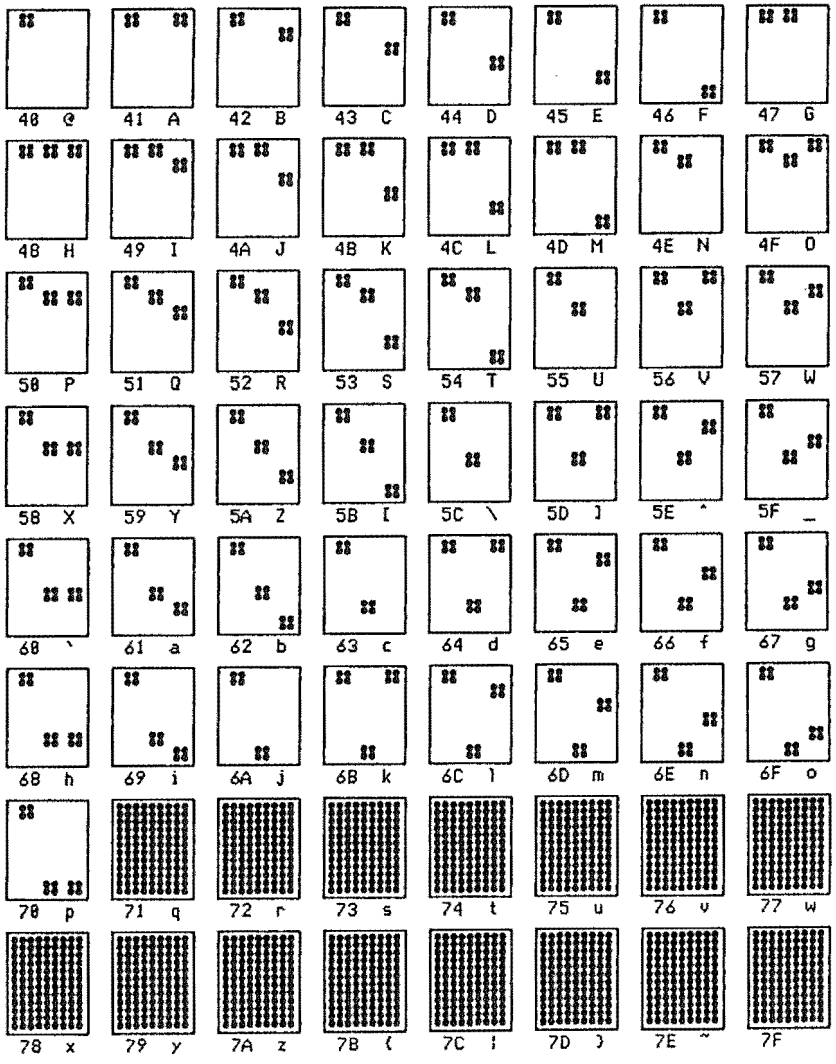
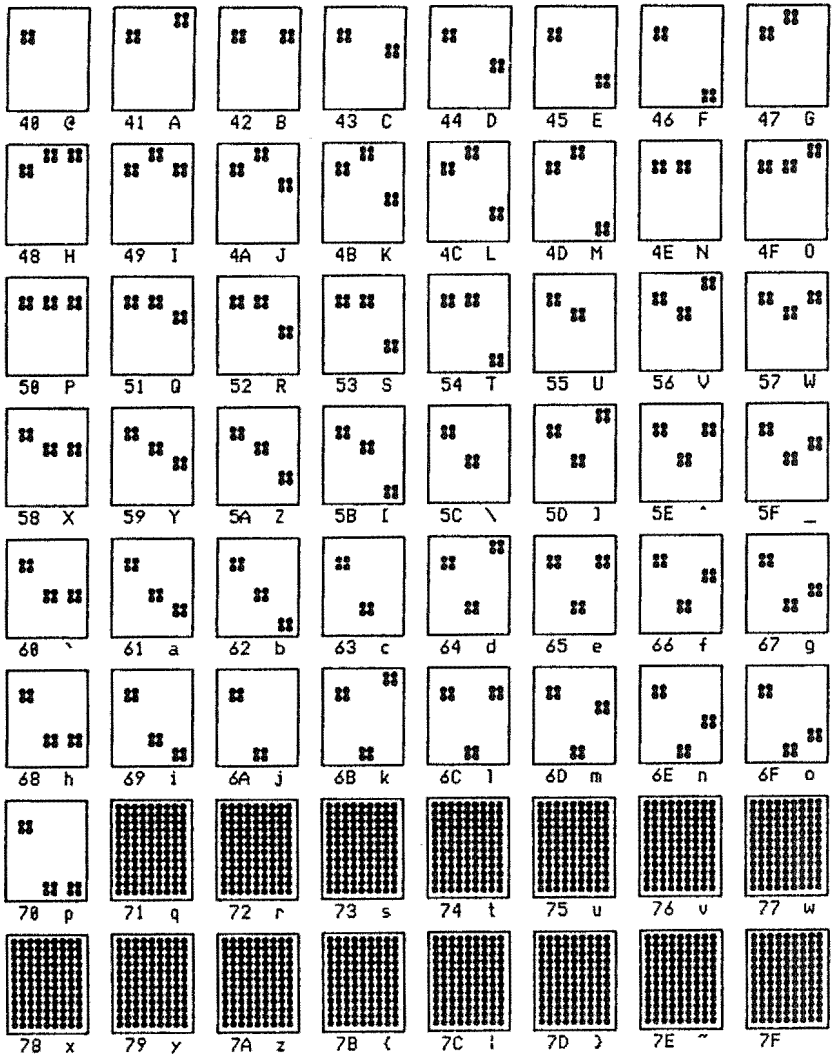
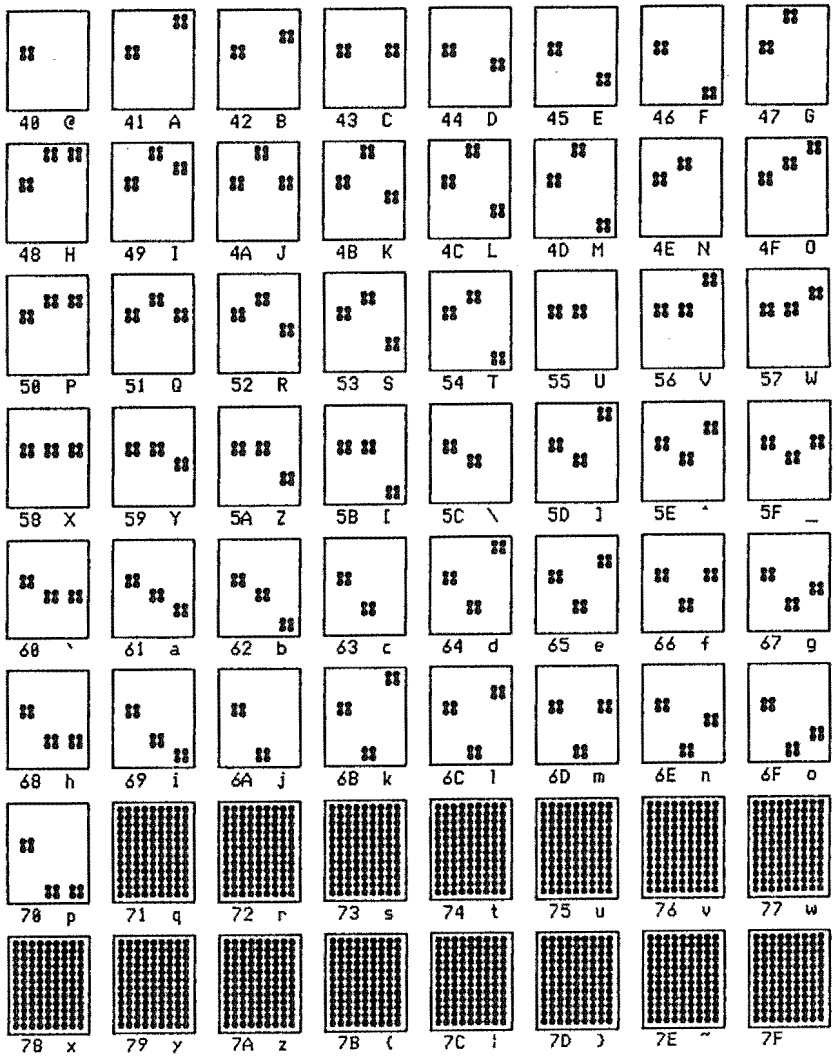


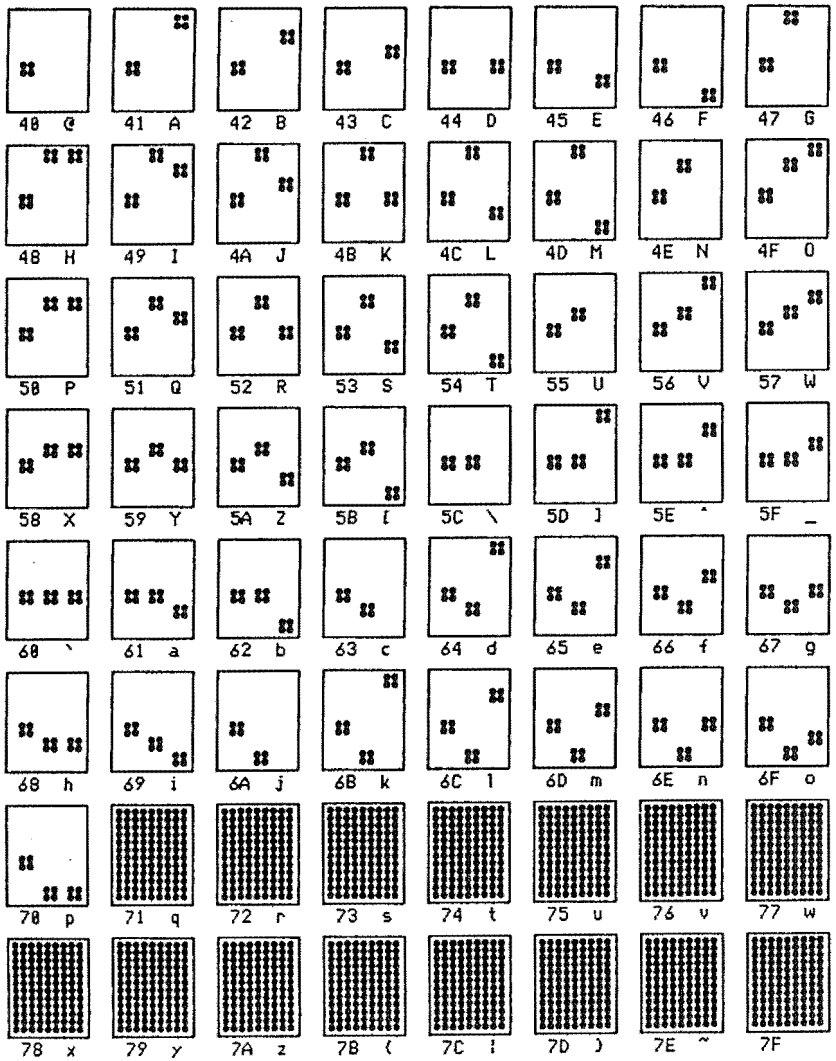
CHARACTER SET #5



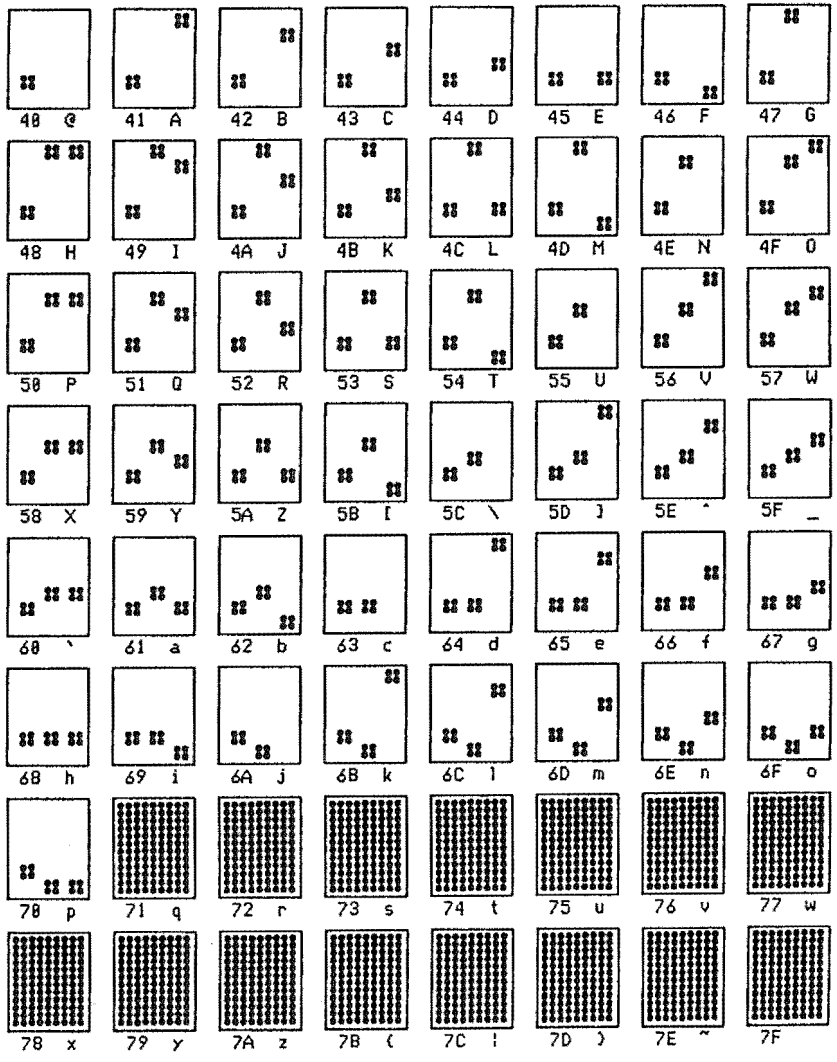
CHARACTER SET #6



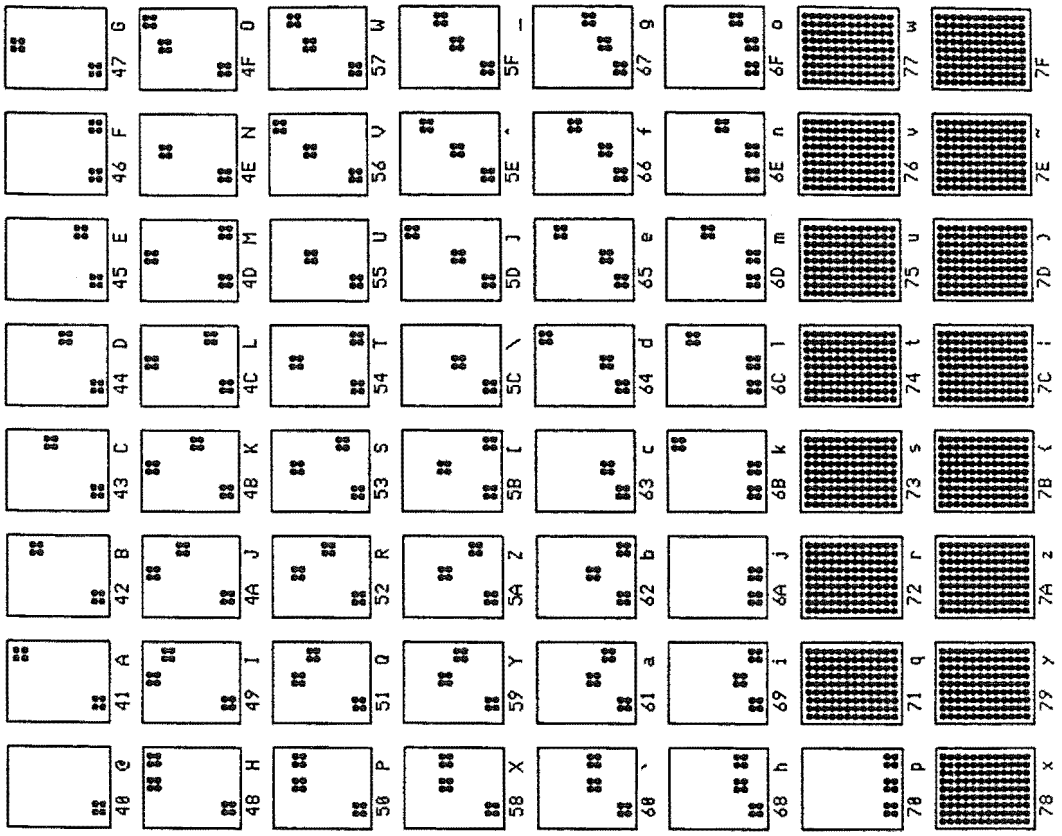
CHARACTER SET #7



CHARACTER SET #8

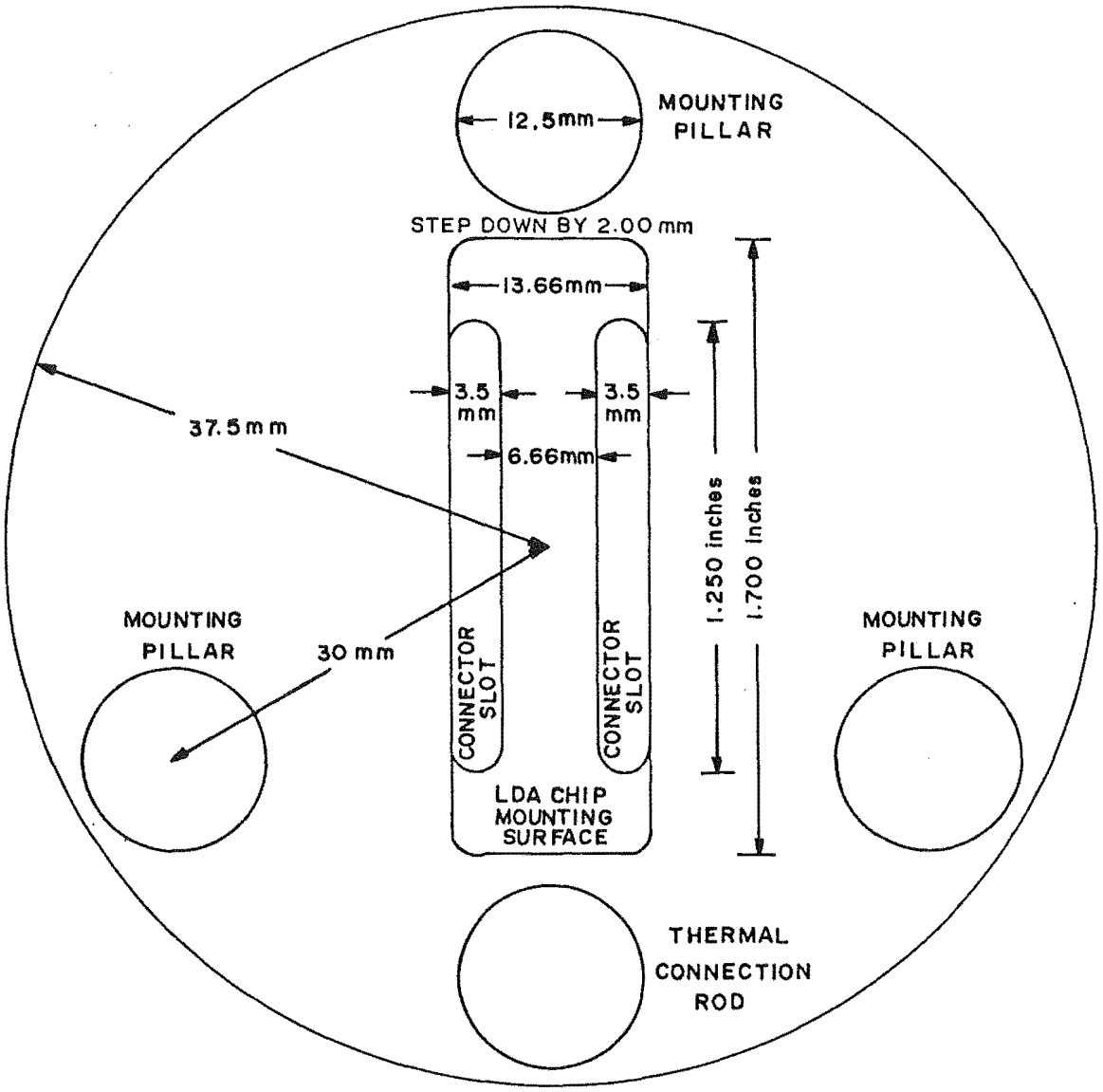


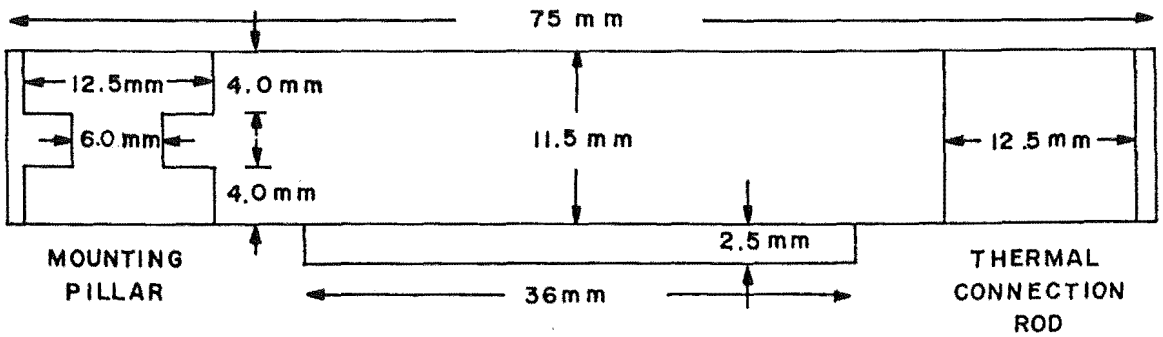
CHARACTER SET #9



APPENDIX TEN

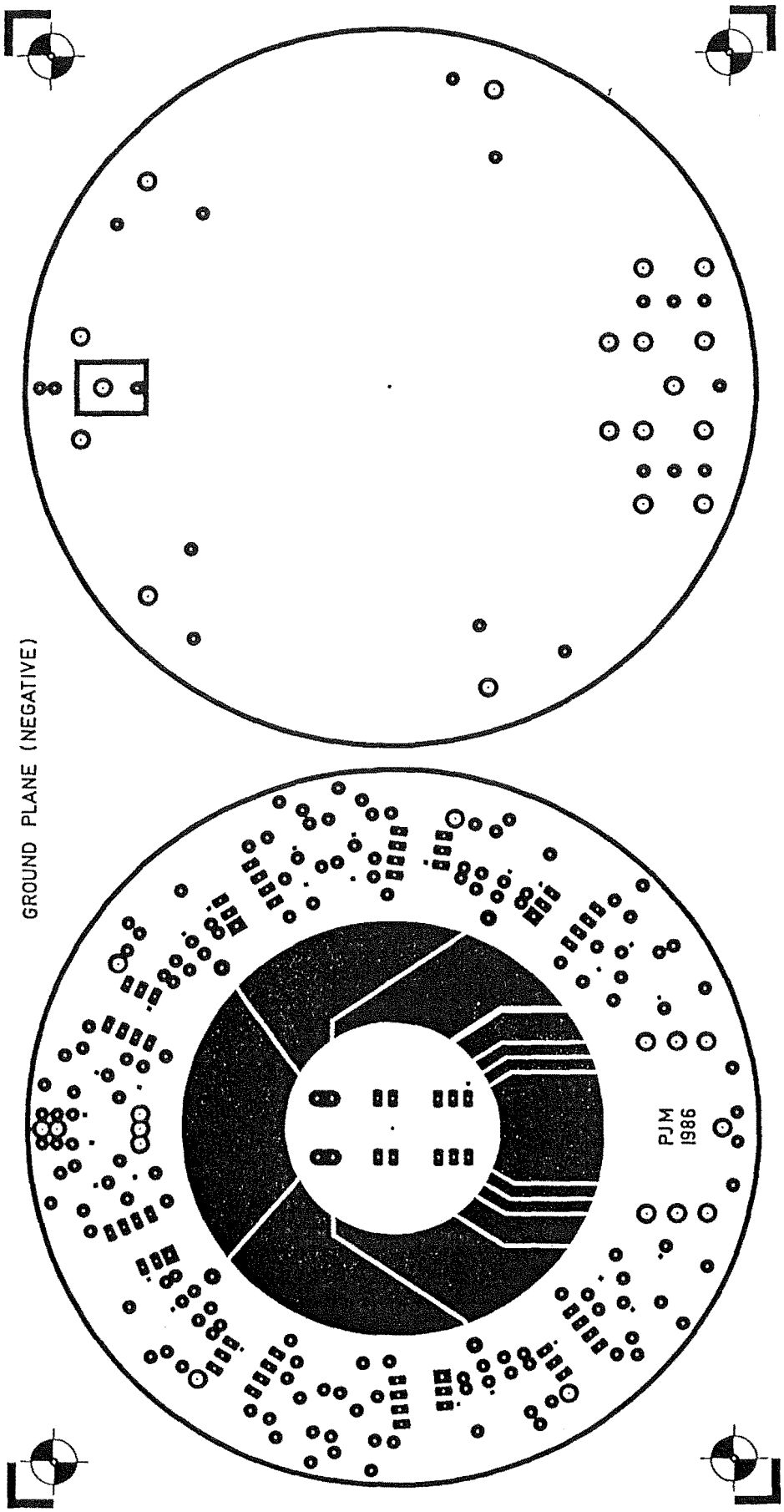
THE LDA MOUNTING BLOCK

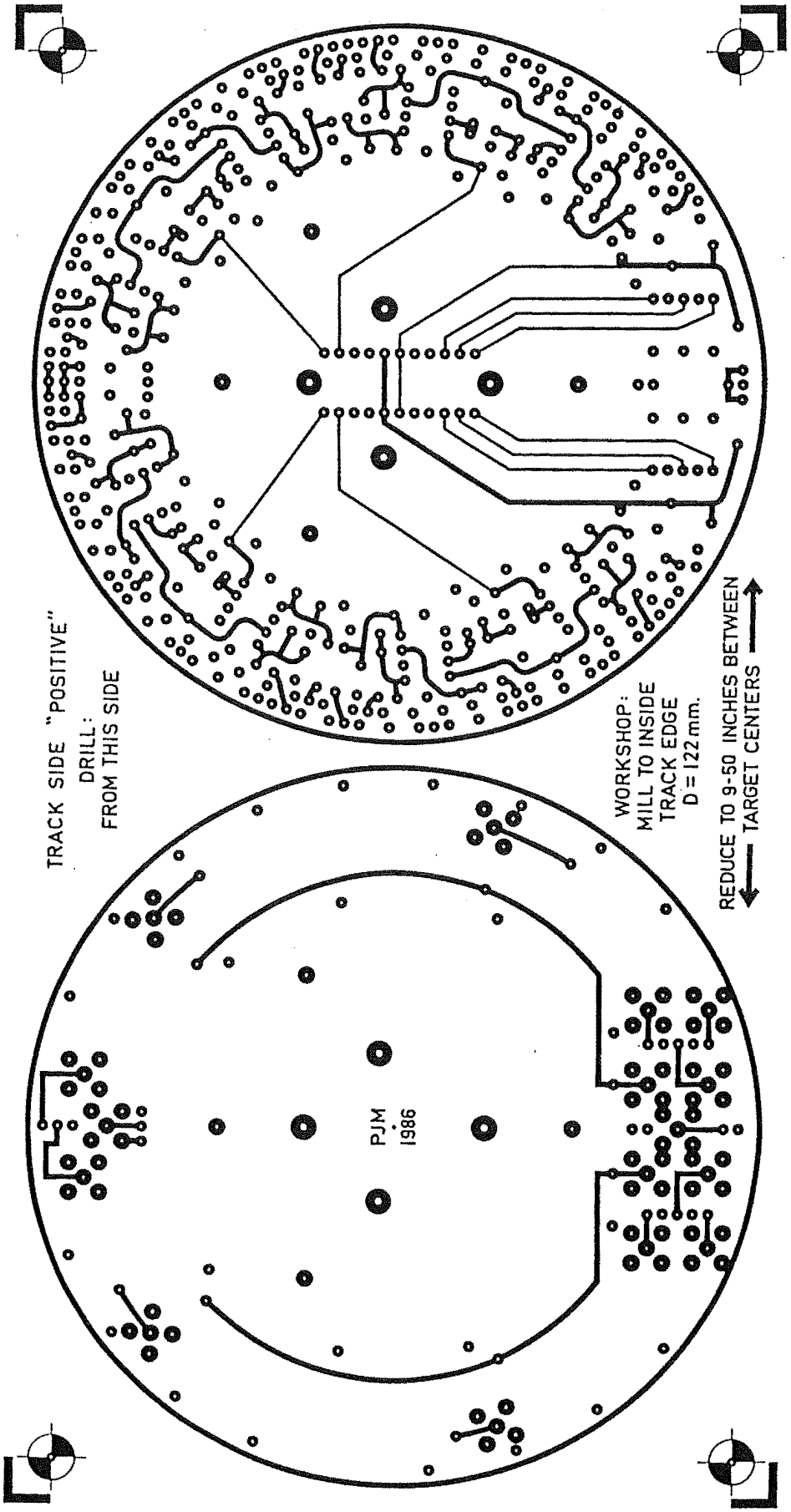




APPENDIX ELEVEN

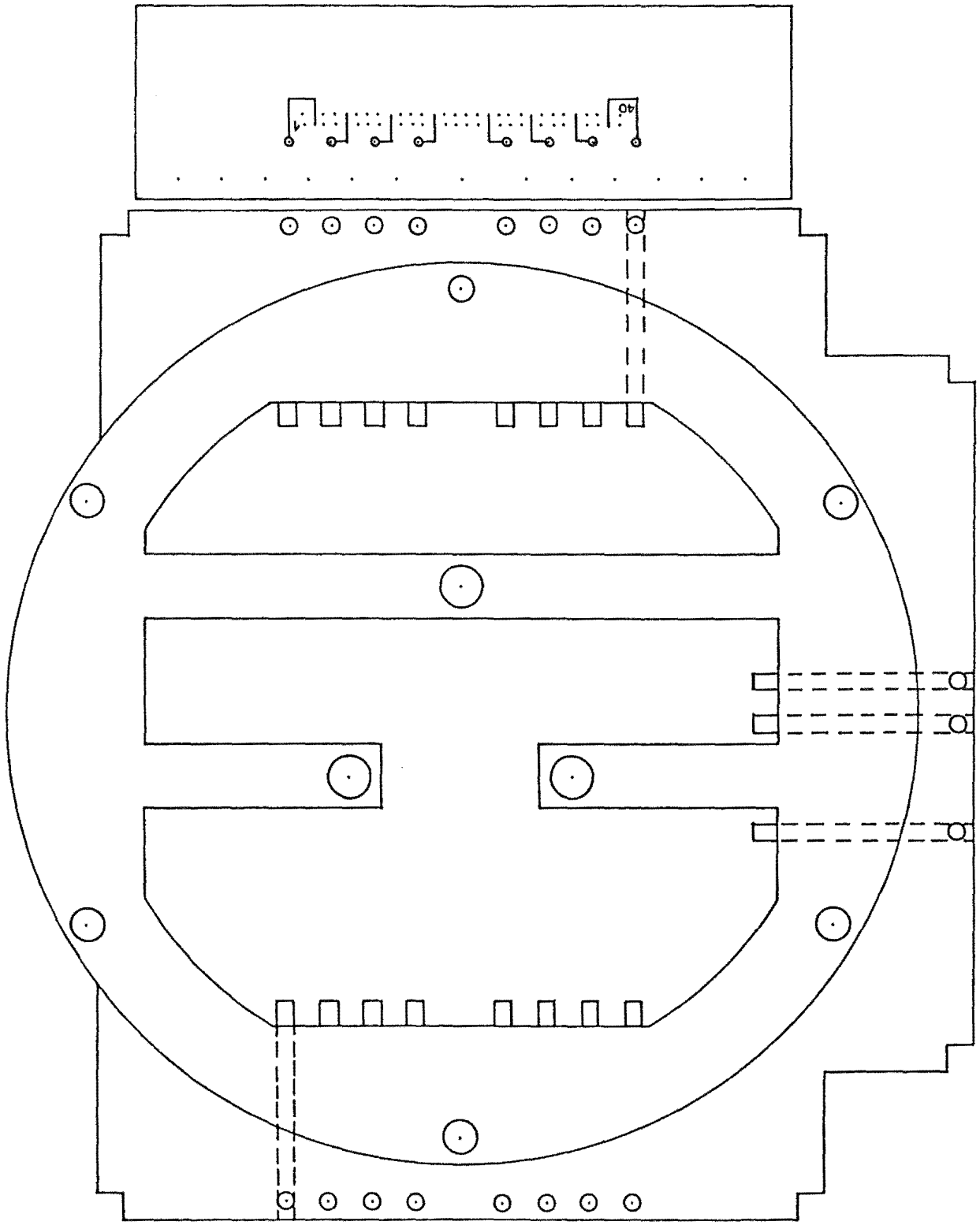
THE PREAMPLIFIER PRINTED CIRCUIT BOARDS




TRACK SIDE "POSITIVE"
DRILL:
FROM THIS SIDE
WORKSHOP:
MILL TO INSIDE
TRACK EDGE
D = 122 mm.
REDUCE TO 9-50 INCHES BETWEEN
TARGET CENTERS
PJM
1986

APPENDIX TWELVE

THE DEWAR FLANGE PLATE



APPENDIX THIRTEEN

PROGRAMME BSY38NSE LISTING

```
PROGRAM BSY38NSE (Input, Output, Auxout) ;
{ This programme calculates the noise voltage amplitude from a BSY38        }
{ transistor after it has had both the transfer function of a differentiator}
{ with a stabilizing pole applied to it, and the transfer function of a     }
{ low-pass filter.  These three time constants are asked for, and the lower }
{ and upper limits of the noise bandwidth.  The integration is performed    }
{ using the trapezium rule, and so the number of divisions into which each  }
{ frequency decade is divided for that integration is also entered.         }
CONST
  PI = 3.1415926 ;
  ESC = #$1B ;
  CR  = #$0D ;
  LF  = #$0A ;
  NULL= #$00 ;
VAR
  TL, TD, TS      : REAL    ;
  H , W , W2      : REAL    ;
  LE, HE, NE      : INTEGER ;
  ND, D , D , N   : INTEGER ;
  A , B , C , IR  : REAL    ;
  F0, F , BC, CC  : REAL    ;
  HINP  , LONP    : REAL    ;
  SUM1  , SUM2    : REAL    ;
  NOISE , TF2     : REAL    ;
  TEMP  , DEN1    : REAL    ;
BEGIN
  {$I+,C+,R+}
  writeln(ESC,'EBSY 38 NOISE CALCULATIONS.',LF) ;
  write('What is the Low-pass filter time constant  ? ');
  readln(TL);
  write('What is the differentiator time constant   ? ');
  readln(TD);
  write('What is the stabilizing pole time constant ? ');
  readln(TS);
  writeln;
  write('What is the exponent of the lower frequency bound  ? ');
  readln(LE);
  write('What is the exponent of the higher frequency bound ? ');
  readln(HE);
  write('How many integrating elements per frequency decade ? ');
  readln(NE);
  write(LF,'Calculating ... ');
  SUM1 := 0 ;
  ND := HE - LE ;
  LONP := 4.9E-09 * 7.656E+07 ;
  HINP := 4.9E-10 * 7.656E+07 ;
  B  := TD + TS ;
  C  := TS + TL ;
  BC := B * C   ;
  CC := C * C   ;
```

(continued)

```
  FOR D := 1 TO ND DO
    BEGIN
      SUM2 := 0 ;
      F0 := 10**(LE-1+D) ;
      H  := 9*F0/NE ;
      FOR N := 1 TO NE DO
        BEGIN
          F := F0 + H*(N-0.5) ;
          W := 2*PI*F ;
          W2 := W*W   ;
          IF F0*10 > 10
            THEN
              IR := HINP
            ELSE
              IR := LONP/F ;
          A  := 1 - W2*TS*TL ;
          DEN1 := A*A + W2*CC ;
          TEMP := SQR(A+W2*BC)/DEN1 + SQR(B*A-C)/DEN1*W2 ;
          TF2  := TEMP / DEN1 ;
          SUM2 := SUM2 + IR * TF2
        END;
      SUM1 := SUM1 + H*SUM2
    END;
  NOISE := SQRT(SUM1);
  write(auxout,ESC,'c1',NULL,ESC,'L008',CR);
  writeln(auxout,'The following result is the r.m.s. voltage noise',
                 ' across a');
  writeln(auxout,'BSY 38 transistor while at a temperature of -130',
                 ' celcius,');
  writeln(auxout,'due to the current noise of an LM 334 current source');
  writeln(auxout,'biasing the BSY 38 with a 100 microamp constant current.');
  writeln(auxout);
  writeln(auxout,'The noise is that which passes the response window');
  writeln(auxout,'of a network comprising the sum of a low-pass filter');
  writeln(auxout,'and that filter followed by a differentiator with a');
  writeln(auxout,'high frequency pole for stabilization.  The relavant');
  writeln(auxout,'time constants are:');
  writeln(auxout);
  writeln(auxout,'      Low-pass filters time constant :',TL:5:2);
  writeln(auxout,'      Differentiators  time constant :',TD:5:2);
  writeln(auxout,'      Stabilizing pole time constant :',TS:5:2);
  writeln(auxout,LF);
  writeln(auxout,'      **********************************');
  writeln(auxout,'      Voltage Noise =',NOISE:7:3,' microvolts');
  writeln(auxout,'      **********************************');
  writeln(auxout,CR,LF);
  writeln(auxout,'This result was calculated using the trapezium rule for');
  writeln(auxout,'the integration. The frequency range for the integration');
  writeln(auxout,'was between 10 ^ ',LE:2,' and 10 ^ ',HE:1,' hertz, and ',
                 'each frequency');
  writeln(auxout,'decade was divided into',NE:3,' integrating elements.');
  writeln(auxout,ESC,'c1',NULL);
  writeln('Finished.')
END.
```

APPENDIX FOURTEEN

PROGRAMME TC_STP_R LISTING

```
PROGRAM Step response (INPUT,OUTPUT,AUXOUT) ;
{ This programme calculates the response of a temperature controller to a   }
{ unity amplitude input step in its reference temperature.                  }
{ INPUT the servo loop time constants : TB,TH,TS,TL, and TT.                }
{ You are then given the critical gain and frequency.                       }
{ Now choose your amplifier gain.                                           }
{ Also choose the first, final, and increments in time for the response     }
{ curve.  Lastly choose the fractional accuracy you want the data to have,  }
{ and the number of times each point must settle to that accuracy before    }
{ the summation is terminated.                                              }
CONST
  PI   = 3.1415926 ;
  CR   = #$0D       ;
  LF   = #$0A       ;
  ESC = #$1B        ;
  NULL= #$00        ;
VAR
  TB,TH,TS,TL,TT : REAL ;
  T0,DT,MT,RF,AC : REAL ;
  G ,NO,FC,CO,CG : REAL ;
  T ,N ,SM,ER,TP : REAL ;
  TM,TN,B ,E ,F  : REAL ;
  RE,IM,W ,W2,QU : REAL ;
  OC,CP,LP,TF,LS : REAL ;
BEGIN
  writeln(ESC,'E','CRITICAL PARAMETER CALCULATIONS',LF);
  write('What is the blocks time constant   ? ');
  readln(TB) ;
  write('What is the heaters time constant  ? ');
  readln(TH) ;
  write('What is the Low-pass time constant ? ');
  readln(TL) ;
  write('What is the Differentiators Stabilizing time constant ? ');
  readln(TS) ;
  write('What is the thermometer time constant ? ');
  readln(TT) ;
  CO:=(TB+TH+TS+TL)/(TB*TS*TL + TH*TS*TL + TB*TH*TS + TB*TH*TL);
  FC:=SQRT(CO)/(2*PI);
  CG:=CO*(TB*(TH+TS+TL)+TH*(TS+TL)+TS*TL)-CO*CO*TB*TH*TS*TL-1 ;
  writeln(LF,'The critical gain is ',CG:-8:2);
  writeln('The critical frequency is ',FC:-8:5);
  write(LF,'What will your amplifier gain be ? ');
  readln(G) ;
  writeln(LF,'THE FOLLOWING PARAMETERS SPECIFY THE RESPONSE CURVE.');
  write(LF,'What is the initial time wanted on the curve ? ');
  readln(T0) ;
  write('What time increments are wanted along the curve ? ') ;
  readln(DT);
  write('What is the maximum time wanted on the curve    ? ');
  readln(MT) ;
  write('What is the repetition frequency of the input step wave  ? ');
  readln(RF) ;
  write('What fractional accuracy shall the data points settle to ? ');
  readln(AC) ;
  write('How many times shall they settle before being accepted   ? ');
  readln(NO) ;
```

(continued)

```
  write(auxout,ESC,'C1',NULL,ESC,'L007');
  writeln(auxout,'The table below numerates the response of a temperature');
  writeln(auxout,'controller to a unity step in its reference temperature.');
  writeln(auxout,'The constant within the servo loop are as follows:');
  write(auxout,LF,LF,'     Cooling Block    time constant : ');
  writeln(auxout,INTEGER(TB):4);
  write(auxout,'     Heater Response  time constant : ');
  writeln(auxout,TH:-5:2);
  write(auxout,'     Thermometer      time constant : ');
  writeln(auxout,TT:-5:2);
  write(auxout,'     Low-pass Filters time constant : ');
  writeln(auxout,TL:-5:2);
  write(auxout,'     Stabilizing Pole time constant : ');
  writeln(auxout,TS:-5:2);
  write(auxout,'     Amplifier Gain                 : ');
  write  (auxout,G:-6:1,CR,LF,LF,LF);
  writeln(auxout,'     ***********************************');
  writeln(auxout,'       The Critical Gain  is = ',CG:-8:2);
  writeln(auxout,'       The Critical Freq. is = ',FC:-8:4);
  writeln(auxout,'     ***********************************');
  write  (auxout,LF,LF);
  writeln(auxout,'           ******      *************');
  writeln(auxout,'            Time        Temperature ');
  writeln(auxout,'           ******      *************');
  writeln(auxout);
  T := T0 ;
  REPEAT
    N := 0 ;
    SM:=0 ;
    ER:=1 ;
    OC:=0 ;
    QU:=0 ;
    CP:=1 ;
    REPEAT
      W := 2*PI*(2*N+1)*RF ;
      W2 := W*W ;
      RE:=1-W2*(TB*TH+TS*TL)+W2*W2*TB*TH*TS*TL-W2*(TB*TS+TH*TS+TB*TL+TH*TL);
      IM:=W*(TB+TH+TS+TL)-W*W2*(TB*TS*TL+TH*TS*TL+TB*TH*TS+TB*TH*TL);
      B:=W*TT;
      E:=G+RE;
      F:=IM ;
      TF:=G * SQRT(SQR(E+B*F)+SQR(B*E-F)) / (E*E+F*F);
      LP:=CP ;
      CP:=ARCTAN((B*E-F)/(E+B*F));
      IF CP > LP
        THEN
          QU := QU-1 ;
      TP:=QU*PI+CP ;
      LS:=SM ;
      SM := SM+TF*SIN(W*T+TP)/(2*N+1) ;
      ER := ABS((SM-LS)/SM) ;
      IF ER < AC
        THEN
          OC:=OC+1
        ELSE
          OC:=0;
      N:=N+1
    UNTIL OC = NO ;
    TM:=0.5+2/PI*SM;
    writeln(auxout,'           ',T:5:1,'          ',TM:8:5);
    T := T+DT
  UNTIL T > MT ;
  writeln(auxout);
  write  (auxout,'The step repetition frequency used was ');
  writeln(auxout,RF:-6:4,' hertz');
  writeln(auxout,'and each of the data points settled to a fractional');
  write  (auxout,'accuracy of ',AC:-6:4);
  writeln(auxout,' a total of ',INTEGER(NO):2,' times sequentially');
  writeln(auxout,'before they were accepted.');
  write(auxout,ESC,'c1',NULL)
END.
```